PART NUMBER
RM65-7102(E)

Rockwell

RM 65
DATA SHEET

IEEE-488 BUS INTERFACE MODULE

RM 65

The RM 65 product line is designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

The RM 65 product line uses a motherboard interconnect concept and accepts any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell's AIM 65 Microcomputer for product development and for a broad variety of portable or desktop microcomputer applications.

PRODUCT OVERVIEW

The RM 65 IEEE-488 Bus Interface Module connects an AIM 65 or RM 65 SBC based system to the IEEE-488 General Purpose Interface Bus (GPIB). Complete controller, talker and listener functions, as defined in the IEEE-488, 1978 Standard, are implemented. The module also supports extended addressing and multiple bus controllers. On-board ROM firmware implements all 12 functions specified by the interface standard. Features not defined in the standard, but also supported, include manual talk or listen disable, dual primary addressing, and an external trigger line. Switches select the Device Talk/Listen Address, Enable Dual Primary Addressing Mode, Disable Talk, Disable Listen, and System Controller mode. The bus interface transceivers meet the electrical specifications of the IEEE-488 interface standard. An 8-inch ribbon cable mates the IEEE-488 module to the IEEE-488 bus with a standard 24-pin connector.

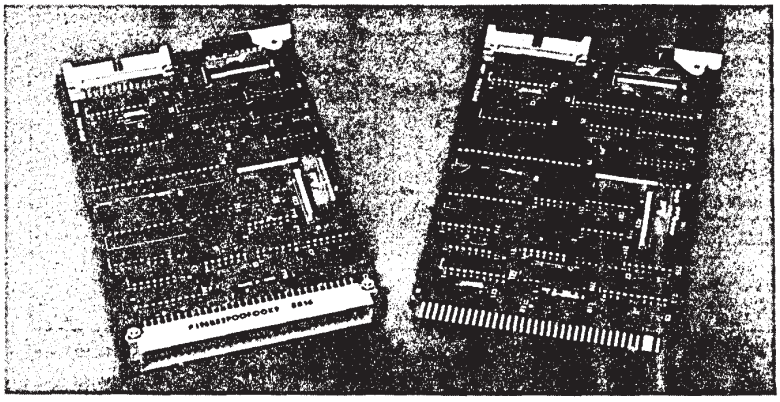
Standard RM 65 features include switches to dedicate the module to one of two 65K byte memory banks, or to assign it common to both banks. A jumper allows the on-board ROM to be enabled or disabled. Base address select switches allow the module I/O address to be assigned to any page (256 bytes) if the ROM is disabled.

ORDERING INFORMATION

The IEEE-488 Bus Interface Module is available in an Edge Connector version (RM65-7102) and a Eurocard version (RM65-7102E).

FEATURES

- Compact size – about 4" x 6½" (100 mm x 160 mm)
- Edge Connector and Eurocard versions
- RM 65 Bus compatible
- Buffered address, data and control lines
- Listen, talk, and controller functions
- IEEE-488, 1978 standard fully implemented
- Uses TI 9914 GPIB Adapter device
- On-board ROM contains bus protocol and utility firmware
- Switches for
  - Device Talk/Listen Address
  - Disable Talk
  - Disable Listen
  - Enable Dual Primary Addressing mode
  - System Controller
  - Base Address to page boundary for I/O
  - Bank Selection to one or both 65K banks
- Jumper for ROM enable/disable
- LEDs show current address register contents
- Supports DMA data transfers
- +5V operation
- Fully assembled, tested and warranted



Eurocard Version
RM65-7102E

Edge Connector Version
RM65-7102

Specifications subject to change without notice
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FUNCTIONAL DESCRIPTION

The Data Transceivers invert and transfer 8-bits of parallel data between the IEEE-488 Bus Interface Module and the RM 65 bus, based on data direction signals from the Base Address Decoder.

The Address Buffers invert and transfer the 16-bit parallel address lines from the RM 65 bus to the Base Address Decoders, to the R2332 ROM and to the GPIB Adapter.

The Control Buffers invert and transfer phase 2 clock, reset, and read/write control signals from the RM 65 bus onto the module. The interrupt request is buffered and driven onto the RM 65 bus.

The Bank Select Control circuit detects when the module's assigned memory bank is addressed by comparing the bank address signal from the RM 65 bus to the Bank Select and Bank Select Enable switches. The Bank Select Enable switch allows the board to reside in common memory (both Bank 0 and Bank 1) or only in the Bank set by the Bank Select switch (either Bank 0 or Bank 1).

The DMA Control circuit allows DMA requests from the TI 9914 GPIB Adapter device to be driven on the RM 65 bus or disabled under program control. This line is jumper selectable for either of two DMA request lines on the RM 65 bus.

The Base Address Decoder compares the eight most significant address lines to the eight Base Address switches. The ROM Disable jumper allows the module to be active in a 4K block when enabled or active in a page (256 locations) when disabled. When an address for the selected bank matches the four most significant switches and the ROM is enabled, the Data Transceivers are enabled and the bus active signal is generated. When this address also matches the four least significant switches the GPIB Adapter and I/O are selected. When there is no match on the four least significant switches, the ROM is selected. When the GPIB Adapter and I/O are selected, the four least significant address lines, phase 2 clocks, and read/write control lines are used to derive register selects for the GPIB Adapter, device selects for the GPIB Status Latch, GPIB Sense Buffers, System Controller Select, and DMA Control Circuits. The read/write control lines also determine the direction for the Data Transceivers.

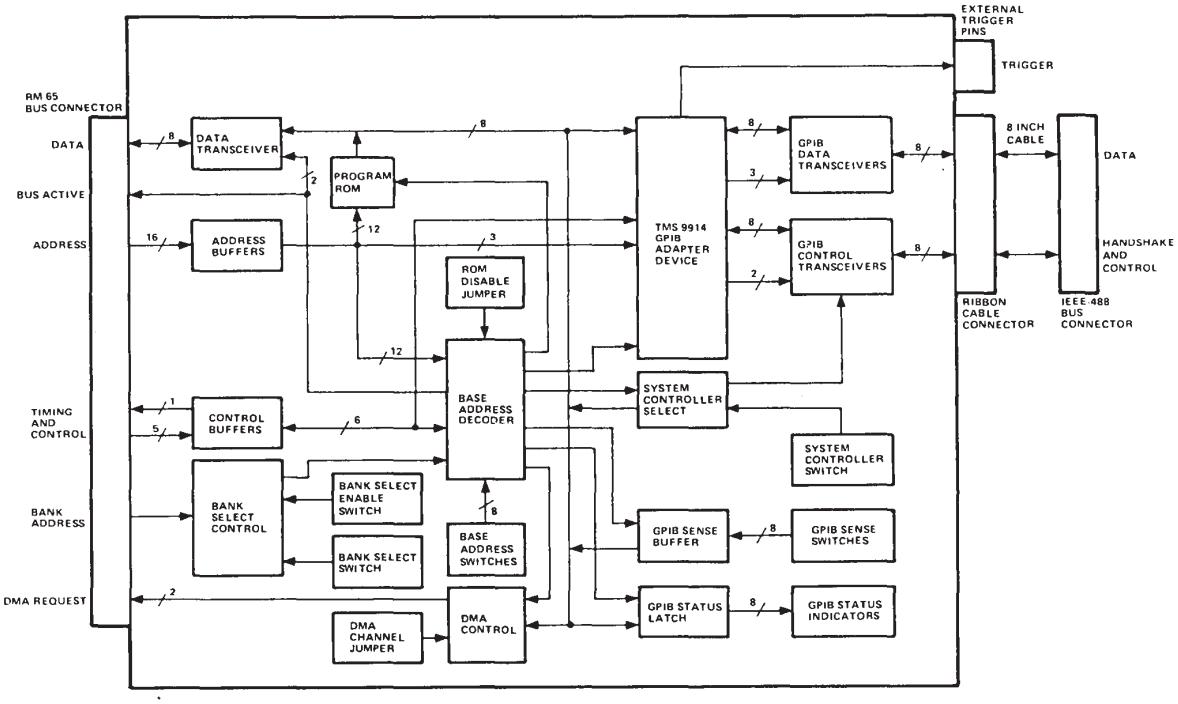
The TMS 9914 GPIB Adapter device provides hardware control of the IEEE-488 bus interface, using firmware subroutines provided in ROM. All bus interface lines are buffered by the GPIB Data and Control Transceivers, to conform to the electrical specifications of the IEEE-488 Standard. These lines are brought out through a cable to a standard IEEE-488 connector. An additional connector provides an external trigger output not defined by the IEEE-488 Standard.

The System Controller Select circuit allows manual selection of System Controller capabilities in multiple controller configurations.

The GPIB Sense Buffer allows the GPIB Sense Switches to be read for Device Talk/Listen Address, Talk or Listen Disable, and Dual Primary Address Mode selection. The GPIB Status Latch latches the positions of the GPIB Sense Switches and displays them on the GPIB Status Indicators. This allows a visual verification of the Device Talk/Listen Address and Operating modes.

On-Board Program ROM Firmware

The Program ROM firmware completely supports all 12 Bus functions described in the IEEE-488, 1978 Standard, as well as features of the TMS 9914 GPIB Adapter device not defined in the Standard. These utility functions make both the Bus protocol and the GPIB Adapter device transparent to the programmer. The firmware, organized as subroutines, is linked to the user program through a jump table. Many of these routines are interrupt-driven, to minimize the processor time in servicing the module. User-alterable vectors and parameters are located in RAM, to allow custom applications. Output data or commands for the Bus are handled as tables, easing the set-up and transfer of information. Extensive error checking by the utility subroutines allow resident or user-provided error handling routines to ensure proper operation of the module, the IEEE-488 Bus and status of data transfer. Two self-test routines verify proper module operation.



IEEE-488 Bus Interface Module Block Diagram

External Trigger Pin Assignments

Pin	Signal Mnemonic	Signal Name	Input/Output
1	TRIG	Trigger Out	O
2	GND	Ground	

IEEE-488 Bus Interface Connector Pin Assignments

Pin	Signal Mnemonic	Signal Name	Input/ Output	Pin	Signal Mnemonic	Signal Name	Input/ Output
1	DI01	Data Input/Output 1	I/O	13	DI05	Data Input/Output 5	I/O
2	DI02	Data Input/Output 2	I/O	14	DI06	Data Input/Output 6	I/O
3	DI03	Data Input/Output 3	I/O	15	DI07	Data Input/Output 7	I/O
4	DI04	Data Input/Output 4	I/O	16	DI08	Data Input/Output 8	I/O
5	EOI	End or Identify	I/O	17	REN	Remote Enable	I/O
6	DAV	Data Available	I/O	18	GND	Ground	N/A
7	NRFD	Not Ready for Data	I/O	19	GND	Ground	N/A
8	NDAC	Not Data Accepted	I/O	20	GND	Ground	N/A
9	IFC	Interface Clear	I/O	21	GND	Ground	N/A
10	SRQ	Service Request	I/O	22	GND	Ground	N/A
11	ATN	Attention	I/O	23	GND	Ground	N/A
12	SHIELD	Ground	N/A	24	GND	Logic Ground	N/A

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Signal Mnemonic	Signal Name	Pin	Pin	Signal Mnemonic	Signal Name
	Not Connected (See Note)	Wa	Wc		Not Connected (See Note)
+5V	+5 Vdc Line (See Note)	Xa	Xc	+5V	+5 Vdc (See Note)
GND	Ground	1a	1c	+5V	+5 Vdc
BADR/	Buffered Bank Address	2a	2c	BA15/	Buffered Address Bit 15
GND	Ground	3a	3c	BA14/	Buffered Address Bit 14
BA13/	Buffered Address Bit 13	4a	4c	BA12/	Buffered Address Bit 12
BA11/	Buffered Address Bit 11	5a	5c	GND	Ground
BA10/	Buffered Address Bit 10	6a	6c	BA9/	Buffered Address Bit 9
BA8/	Buffered Address Bit 8	7a	7c	BA7/	Buffered Address Bit 7
GND	Ground	8a	8c	BA6/	Buffered Address Bit 6
BA5/	Buffered Address Bit 5	9a	9c	BA4/	Buffered Address Bit 4
BA3/	Buffered Address Bit 3	10a	10c	GND	Ground
BA2/	Buffered Address Bit 2	11a	11c	BA1/	Buffered Address Bit 1
BA0/	Buffered Address Bit 0	12a	12c	BØ1	* Buffered Phase 1 Clock
GND	Ground	13a	13c	BSYNC	* Buffered Sync
BSO	* Buffered Set Overflow	14a	14c	BDRQ1/	Buffered DMA Request 1
BRDY	* Buffered Ready	15a	15c	GND	Ground
	* User Spare 1	16a	16c	-12V/-V	* -12 Vdc/-V
+12V/+V	* +12 Vdc/+V	17a	17c		* User Spare 2
GND	Ground	18a	18c	BFLT/	* Buffered Bus Float
BDMT/	* Buffered DMA Terminate	19a	19c	BØ0	* Buffered External Phase 0 Clock
	* User Spare 3	20a	20c	GND	Ground
BR/$\overline{W}$/	Buffered Read/Write "Not"	21a	21c	BDRQ2/	Buffered DMA Request 2
	* System Spare	22a	22c	BR/$\overline{W}$	Buffered Read/Write
GND	Ground	23a	23c	BACT/	Buffered Bus Active
BIRQ/	Buffered Interrupt Request	24a	24c	BNMI/	* Buffered Non-Maskable Interrupt
BØ2/	Buffered Phase 2 "Not" Clock	25a	25c	GND	Ground
BØ2	Buffered Phase 2 Clock	26a	26c	BRES/	Buffered Reset
BD7/	Buffered Data Bit 7	27a	27c	BD6/	Buffered Data Bit 6
GND	Ground	28a	28c	BD5/	Buffered Data Bit 5
BD4/	Buffered Data Bit 4	29a	29c	BD3/	Buffered Data Bit 3
BD2/	Buffered Data Bit 2	30a	30c	GND	Ground
BD1/	Buffered Data Bit 1	31a	31c	BD0/	Buffered Data Bit 0
+5V	+5 Vdc	32a	32c	GND	Ground
+5V	+5 Vdc (See Note)	Ya	Yc	+5V	+5 Vdc (See Note)
	Not Connected (See Note)	Za	Zc		Not Connected (See Note)

NOTE

Pins Wa, Wc, Xa, Xc, Ya, Yc, Za and Zc are not used on Eurocard version.

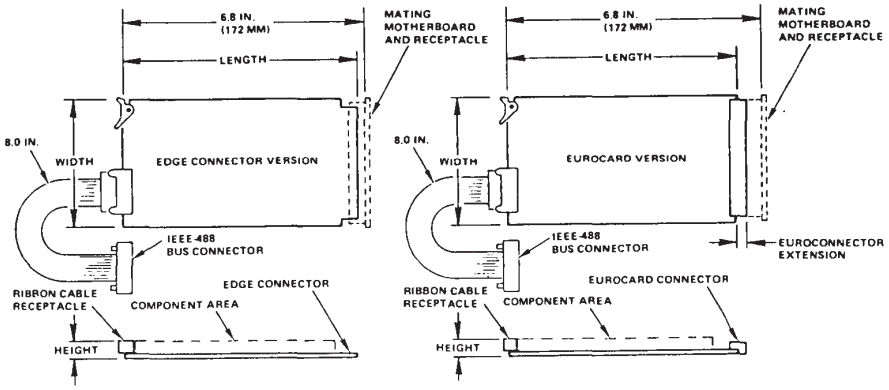
* Not used on this module.

IEEE-488 Bus Interface Module Physical and Electrical Characteristics

Characteristic	Value	
Physical Characteristics (See Notes)	Edge Connector	Eurocard
Width	3.9 in. (100 mm)	3.9 in. (100 mm)
Length	6.5 in. (164 mm)	6.3 in. (160 mm)
Height	0.56 in. (14 mm)	0.56 in. (14 mm)
Weight	4.6 oz. (130 g)	5.0 oz. (140 g)
Environment		
Operating Temperature	$0^{o}C$ to $70^{o}C$	
Storage Temperature	$-40^{o}C$ to $+85^{o}C$	
Relative Humidity	0% to 85% (without condensation)	
Power Requirements	+5 Vdc ±5% @ 0.65A (3.25W) -- Typical 1.0A (5.25 W) -- Maximum	
RM 65 Bus Interface		
Edge Connector Version	72-pin edge connector (0.100 in. centers)	
Eurocard Version	64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed)	
Module		
I/O Interface		
Cable Receptacle	26-pin mass terminated (0.100 in. centers)	
Trigger Connector	Two vertical wire wrap pins (0.3 in. high on 0.200 in. centers)	
IEEE-488 Bus Interface Cable		
IEEE-488 Bus Connector	24-pin mass terminated (2.16 mm centers) with metric thread lock screws (Amphenol 57 or equivalent)	
Module Connector	26-pin mass terminated (0.100 in. centers)	
Cable Length	8 inches	
Type	Flat ribbon	
Number of Conductors	24	
Wire Size	#28 AWG	

NOTES:

1. The height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. The length does not include the added extension due to the module ejector
3. The Eurocard dimensions conform to DIN 41612.



Module Dimensions