Rockwell

RM65-5223E
RM 65 MULTI-FUNCTION PERIPHERAL INTERFACE MODULE

RM 65 MICROCOMPUTER MODULES

The RM65-5223E Multi-Function Interface (MPI) Module is one of the hardware options available for the RM 65 Microcomputer Module family.

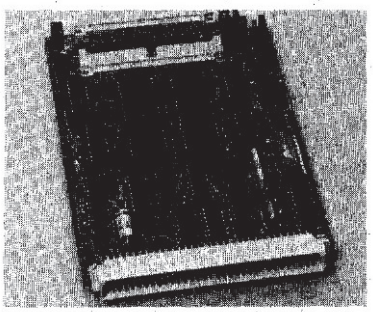
RM 65 Microcomputer Modules products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 modules use a motherboard interconnect concept and accept any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and for a broad variety of portable or desk-top microcomputer applications.

PRODUCT OVERVIEW

The RM65-5223E RM 65 Multi-function Interface (MPI) Module provides a parallel I/O interface to the RM 65 Bus. Two R6522 Versatile Interface Adapter (VIA) devices provide four 8-bit bidirectional data ports and four 2-bit control ports; 40 I/O lines in all. Two multi-mode 16-bit timer/counters extend the versatility of the module. All I/O lines are TTL buffered and available on two 40 pin I/O connectors compatible with the AIM 65/40 SBC and RM 65 SBC Parallel Application connectors. Data buffer direction is under direct software control. Twelve jumpers specify the direction of the control lines, while an additional 6 jumpers control the optional features.

The MPI Module I/O can be assigned either to one of two 65K byte memory banks or common to both banks. Eight switches allow I/O addresses to be set to any page (256 bytes).



RM65-5223E Multi-function Peripheral Interface (MPI) Module

FEATURES

- Compact size—about 4" × 6¼" (100 mm × 160 mm)
- Pin and socket bus connection
- RM 65 Bus compatible
- Two R6522 Versatile Interface Adapter (VIA) devices
- Four fully buffered 8-bit parallel data ports
- Four fully buffered 2-bit control ports
- Four programmable 16-bit counter/timers
- Two serial input/output ports
- Multiple interrupt conditions
- Full buffering on all I/O data and control lines
- Software-controlled data line direction
- Jumper-selectable control line direction
- Data port buffering can be removed
- All I/O lines are available on two 40-pin I/O connectors
- I/O connectors are compatible with both the AIM 65/40 and RM 65 SBC module parallel I/O connectors and AIM 65/40 intelligent peripherals
- One connector is fully compatible with the AIM 65/40 standard or extended keyboard
- Bank switches assign I/O addresses to one or two 65K banks
- I/O base address switch selectable to a page boundary
- +5V operation
- Fully assembled, tested and warranted

ORDERING INFORMATION

Part No.	Description
RM65-5223E	Multi-function Peripheral Interface (MPI) Module
Order No.	**Description**
817	Multi-function Peripheral Interface Module (MPI) Module User's Manual (included with RM65-5223E)

FUNCTIONAL DESCRIPTION

The heart of the MPI module is two R6522 Versatile Interface Adapter (VIA) devices. Each VIA provides two 8-bit bidirectional input/output ports, four I/O control lines, two fully programmable 16-bit timer/counters and an 8-bit shift register for serial interface. There is also control of interrupt generation from independent I/O conditions.

The two 8-bit input/output peripheral ports are fully bidirectional. Data direction registers allow each peripheral pin to independently act as either an input or an output. The four control lines can also be used for I/O or can provide handshaking for the associated data ports. Each control input can be programmed to interrupt the microprocessor on detection of a rising or falling edge.

The two 16-bit counter/timers are capable of many complex timing and counting functions. One timer provides four modes of operation: free running, with pulsed or toggled output, one-shot interval timer with a low-level output on a peripheral port line, or one-shot interval timer with a toggle output on a peripheral port line. The three modes of the second 16-bit timer provide a one-shot interval timer, a count of external pulses, or a clock for serial shift register. The shift register can shift in, or shift out data at the system clock rate, the timer clock rate, or an external clock rate. Both timers and the shift register can be programmed to interrupt the microprocessor upon time-out or shift completion.

Four Port Transceivers buffer the VIA data lines for input or output modes. The I/O Data Direction Control logic allows the direction of each 8-bit port to be independently set for input or output mode under software controls. In the buffered output mode, the Port Transceivers are capable of sinking 16 mA on any data line. For applications where buffering is not desired, any of the Port Transceivers can be replaced with DIP shunts for direct connection to the VIA peripheral data pins.

The I/O Control Signal Buffers fully buffer all eight VIA Control lines. On each VIA, one control line (CA1) has only an input mode which is buffered as such. Twelve I/O Control Direction Jumpers allow the three bidirectional control lines (CA2, CB1, and CB2) on each R6522 to be configured for either input or output mode.

A number of options available on VIA No. 1 make it particularly well-suited for keyboard applications. The A port of VIA No. 1 is supplemented with Line Low Detection circuitry which generates an interrupt through control line CA1 when any line goes low; a reset switch on control line CB2 is passed off the board from the RESET connector to be used by reset conditioning circuitry on an RM 65 SBC module, AIM 65 micocomputer or AIM 65/40 SBC module; an attention switch on control line CB1 is debounced by the Attention Interrupt Conditioning circuitry to generate a non-maskable interrupt when enabled by the Attention Interrupt jumper.

Two 40-pin Parallel I/O connectors support all the R6522 VIA signals as well as the Attention and Reset switch options. These connectors can be configured to match the RM 65 or AIM 65/40 SBC module Parallel Application connectors, while also being compatible with AIM 65/40 peripherals—keyboard, display or printer. The I/O Power Source jumpers allow +5V to be supplied to the interfacing equipment through the Parallel I/O Connector.

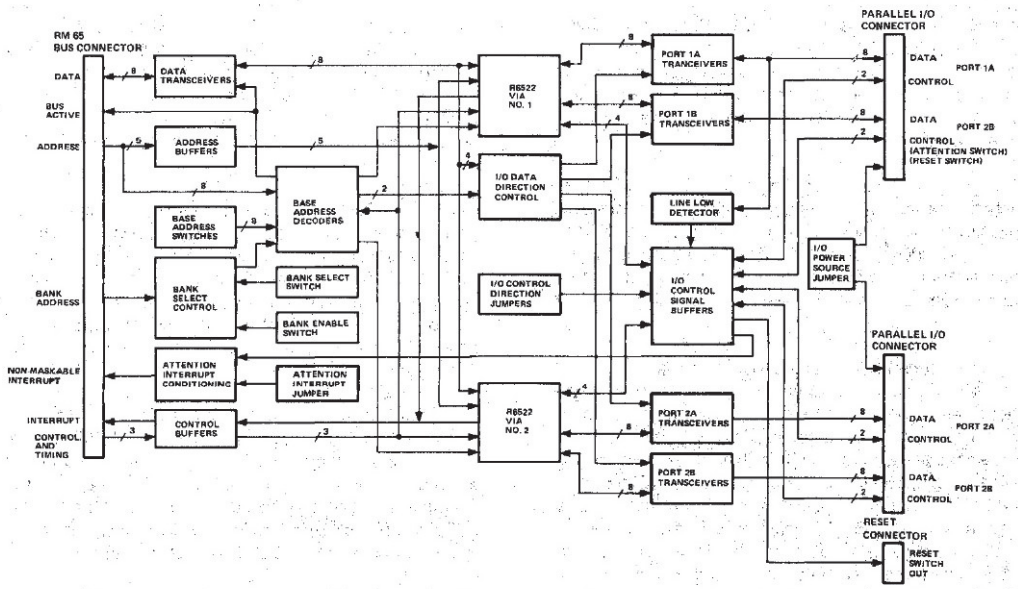
The Data Transceivers invert and buffer 8-bits of parallel data between the RM 65 Bus and the two R6522 VIA devices or the I/O Direction Control logic. The Data Transceivers are enabled when a valid address is present at the Base Address Decoders. During a read operation, data is transferred from the addressed I/O to the RM 65 Bus. During a write operation, data is transferred from the RM 65 Bus to the addressed I/O.

The Address Buffers invert the six least significant address bits used to select the R6522 devices and registers and also the I/O Direction Control Logic.

The Control Buffers drive read/write, phase 2 clock, and reset signals from the RM 65 Bus to the MPI module. The interrupt request and bus active signals are driven from the MPI module.

The Bank Select Control circuit detects when the MPI module's assigned memory bank is addressed by comparing the bank address signal from the RM 65 Bus to the Bank Select Enable and Bank Select switches. The Bank Select Enable switch allows the module to be assigned either common to both banks, or to Bank O (lower 65K) or Bank 1 (upper 65K) depending on the Bank Select switch.

The Base Address Decoders use the eight most significant address lines to assign the MPI module to a page (256 bytes) boundary. When an address is within range of the Base Address switches and the Bank Control is enabled, a chip select is generated to one of the R6522 devices or the I/O Direction Control logic is selected.



MPI Module Block Diagram

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Pin	Signal Mnemonic	Signal Name	Pin	Signal Mnemonic	Signal Name
1a	GND	Ground	1c	+5V	+5 Vdc
2a	BADR/	Buffered Bank Address	2c	BA15/	Buffered Address Bit 15
3a	GND	Ground	3c	BA14/	Buffered Address Bit 14
4a	BA13/	Buffered Address Bit 13	4c	BA12/	Buffered Address Bit 12
5a	BA11/	Buffered Address Bit 11	5c	GND	Ground
6a	BA10/	Buffered Address Bit 10	6c	BA9/	Buffered Address Bit 9
7a	BA8/	Buffered Address Bit 8	7c	BA7/	*Buffered Address Bit 7
8a	GND	Ground	8c	BA6/	*Buffered Address Bit 6
9a	BA5/	Buffered Address Bit 5	9c	BA4/	Buffered Address Bit 4
10a	BA3/	Buffered Address Bit 3	10c	GND	Ground
11a	BA2/	Buffered Address Bit 2	11c	BA1/	Buffered Address Bit 1
12a	BA0/	Buffered Address Bit 0	12c	BØ1	*Buffered Phase 1 Clock
13a	GND	Ground	13c	BSYNC	*Buffered Sync
14a	BSO	*Buffered Set Overflow	14c	BDRQ1/	*Buffered DMA Request 1
15a	BRDY	*Buffered Ready	15c	GND	Ground
16a		*User Spare 1	16c	−12V/−V	*−12 Vdc/−V
17a	+12V/+V	*+12 Vdc/+V	17c		*User Spare 2
18a	GND	Ground Line	18c	BFLT/	*Buffered Bus Float
19a	BDMT/	*Buffered DMA Terminate	19c	BØ0	*Buffered External Phase 0 Clock
20a		*User Spare 3	20c	GND	Ground
21a	BR/$\overline{W}$/	Buffered Read/Write "Not"	21c	BDRQ2/	*Buffered DMA Request 2
22a		*System Spare	22c	BR/$\overline{W}$	*Buffered Read/Write
23a	GND	Ground	23c	BACT/	Buffered Bus Active
24a	BIRQ/	Buffered Interrupt Request	24c	BNMI/	Buffered Non-Maskable Interrupt
25a	BØ2/	Buffered Phase 2 "Not" Clock	25c	GND	Ground
26a	BØ2	*Buffered Phase 2 Clock	26c	BRES/	Buffered Reset
27a	BD7/	Buffered Data Bit 7	27c	BD6/	Buffered Data Bit 6
28a	GND	Ground	28c	BD5/	Buffered Data Bit 5
29a	BD4/	Buffered Data Bit 4	29c	BD3/	Buffered Data Bit 3
30a	BD2/	Buffered Data Bit 2	30c	GND	Ground
31a	BD1/	Buffered Data Bit 1	31c	BD0/	Buffered Data Bit 0
32a	+5V	+5 Vdc	32c	GND	Ground

Note:
*Not used on this module.

Connector J1 and J2 (Parallel I/O Connector) Pin Assignments

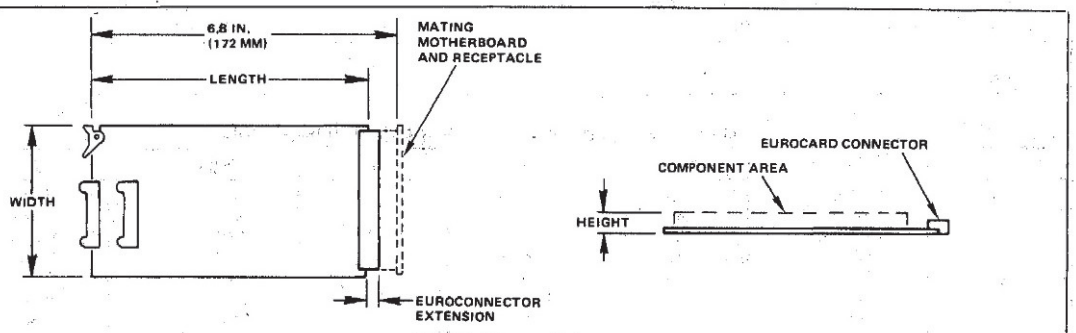
Pin	Signal	I/O	Type	Pin	Signal	Type
1	CB2/$\overline{RES}$	I/O	NMOS	2	GND/+5V*	Power
3	CB1/$\overline{ATTN}$	I/O	NMOS	4	GND	Power
5	PB7	I/O	NMOS	6	GND	Power
7	PB6	I/O	NMOS	8	GND	Power
9	PB5	I/O	NMOS	10	GND	Power
11	PB4	I/O	NMOS	12	GND	Power
13	PB3	I/O	NMOS	14	GND	Power
15	PB2	I/O	NMOS	16	GND	Power
17	PB1	I/O	NMOS	18	GND	Power
19	PB0	I/O	NMOS	20	GND	Power
21	PA7	I/O	NMOS	22	GND	Power
23	PA6	I/O	NMOS	24	GND	Power
25	PA5	I/O	NMOS	26	GND	Power
27	PA4	I/O	NMOS	28	GND	Power
29	PA3	I/O	NMOS	30	GND	Power
31	PA2	I/O	NMOS	32	GND	Power
33	PA1	I/O	NMOS	34	GND	Power
35	PA0	I/O	NMOS	36	GND	Power
37	CA2	I/O	NMOS	38	GND	Power
39	CA1	I	NMOS	40	GND/+5V*	Power

Notes:
1. Pins 2 and 40 can be optionally jumpered to +5V (maximum current through each pin should not exceed 200 mA).
2. Pin 1 of J1 can be optionally jumpered to RESET connector or to CB2.
3. Pin 3 of J1 can be optionally jumpered to the Attention Interrupt Conditioning circuit or to CB1.

SPECIFICATIONS

Parameter	Value
Dimensions (1, 2, 3)	
Width	3.9 in. (100 mm)
Length	6.3 in. (160 mm)
Height	0.56 in. (14 mm)
Weight	5.1 oz. (145 g)
Environment	
Operating Temperature	0°C to 70°C
Storage Temperature	−40°C to +85°C
Relative Humidity	0% to 85% (without condensation)
Power Requirements	+5 Vdc ±5% 0.65 A (3.25 W)—Typical +5 Vdc ±5% 1.03 A (5.15 W)—Maximum
Interfaces	
RM 65 Bus Interface	64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed)
I/O Interface	
Parallel I/O Connectors (2)	40-pin 3M #3495-1002, or equivalent, receptacle. Mates with 3M #3418-0000T, or equivalent, ribbon cable connector
Reset Connector	2 vertical pins (0.3 in. high) on 0.200 in. center

Notes:
1. Height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. Length does not include extensions beyond the edge of the module due to connectors or the module ejector.
3. Dimensions conform to DIN 41612.



Module Dimensions