



RM65-5102E RM 65 CRT CONTROLLER (CRTC) MODULE

RM 65 MICROCOMPUTER MODULES

The RM65-5102E CRT Controller Module is one of the hardware options available for the RM 65 Microcomputer Module family.

RM 65 Microcomputer Module products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 modules use a motherboard interconnect concept and accept any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and for a broad variety of portable or desktop microcomputer applications.

PRODUCT OVERVIEW

The CRT Controller (CRTC) Module interfaces the RM 65 to a CRT monitor or television receiver. The CRTC module outputs HSYNC, VSYNC, and raw video signals for direct connection to a CRT Monitor, and composite video for connection to a CRT monitor or to a TV receiver through an RF modulator. A socketed on-board ROM generates 5 × 7 characters with two descenders in a 7 × 10 dot matrix field to provide upper and lower case alphanumeric and special symbols. The 2K bytes of on-board display RAM are memory-mapped.

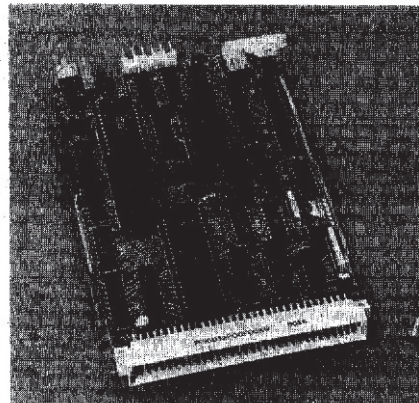
A 2K-byte program ROM provides firmware to configure the display format for 80 columns by 25 rows or 40 columns by 16 rows, scan rate of 50 or 60 Hz, and a CRT display driver for AIM 65. There are also cursor control, screen editing, and utility routines.

ORDERING INFORMATION

Part No.	Description
RM65-5102E	CRT Controller (CRTC) Module
Order No.	Description
814	CRT Controller (CRTC) Module User's Manual (included with RM65-5102E)

FEATURES

- Compact size—about 4" × 6¼" (100 mm × 160 mm)
- RM 65 bus compatible
- 4K Byte character generator ROM with:
 - Upper and lower case alphabets
 - Special characters
 - Numbers including subscripts and superscripts
 - Math symbols
 - Semi-graphics
- On-board ROM firmware supports:
 - Scrolling
 - Screen editing
 - Full cursor movement control
 - Full screen standard or inverse video
 - Predefined formats for
 - 80 column by 25 row (50/60 Hz)
 - 72 column by 22 row (50/60 Hz)
 - 40 column by 25 row (60 Hz)
 - 40 column by 16 row (60 Hz)
 - Selectable format from 1 to 80 columns by 1 to 25 rows
 - NTSC (60 Hz, 525 lines per frame) and European (50 Hz, 625 lines per frame) raster format
 - CRT display driver for AIM 65
- Single 5 volt operation
- Fully assembled, tested and warranted



RM65-5102E CRT Controller (CRTC) Module

FUNCTIONAL DESCRIPTION

The Data Transceivers invert and transfer 8 bits of parallel data between the CRTC Module and the RM 65 bus, based on control signals from the Base Address Decoder and the Control Buffers. The read/write control line determines the direction, while the bus active enables the Data Transceivers.

The Address Buffers invert and transfer the 16-bit parallel address lines from the RM 65 bus to the Base Address Decoders, the R2316 ROM, the CRT Controller (CRTC) device, and to the Refresh RAM device.

The Control Buffers invert and transfer the phase 2 clock and read/write control signals from the RM 65 bus onto the module.

The Bank Select Control circuit detects when the module's assigned memory bank is addressed, by comparing the bank address signal from the RM 65 bus to the Bank Select and Bank Select Enable switches. The Bank Select Enable switch allows the board to reside in common memory (both Bank 0 and Bank 1) or only in the Bank set by the Bank Select switch (either Bank 0 or Bank 1).

The Base Address Decoder, with the Base Address Select switches, the Bank Select Control circuit, the ROM Disable Switch and the read/write and phase 2 clock signals, generates device selects for the on-board ROM, RAM, and I/O (CRTC device and Display Enable Status Buffer). The Base Address Select switches allow the module to be selected to any 4K block. Within the selected 4K block, the RAM is assigned to the lower 8 pages (2K bytes), and the I/O to the first 256 byte page of the upper 2K bytes. When the ROM is disabled, only the RAM and I/O can be selected and the module is assigned 9 pages (2304 bytes) in memory. When the ROM is enabled, the module is assigned the full 4K bytes, with 7 pages for ROM, in addition to the RAM and I/O.

The Controller Clock uses a crystal-controlled oscillator to derive a 6 MHz or 12 MHz reference for the shift register dot clock depending on the Dot Clock Select jumper position. With the 6 MHz clock, up to 40 characters per line can be displayed on any monitor or standard television using an RF modulator. Up to 80 characters per line can be achieved with the 12 MHz clock and a high bandwidth monitor. The dot clock is divided by seven to provide a Character Clock for the CRTC device and a load character signal for the shift register.

The Refresh RAM provides 2K bytes of display memory, for screen densities of up to 25 lines with as many as 80 characters each. The RAM is directly mapped into the RM 65 memory map,

so the display can be updated by a block memory move or under DMA control. The Refresh RAM Multiplexer and RAM Transceiver allow the RM 65 bus and the CRTC device to both access the Refresh RAM, with the RM 65 bus having priority when any conflict occurs.

The Display Enable Status Buffer allows the RM 65 bus to monitor the active display times, so that display memory transfers can be made with no visible distortion.

The Character Generator ROM holds the fonts for the character set. These fonts are stored as 256 characters, each with 10 seven-bit rows. The four CRTC device row address lines and the eight Character Latch bits, which hold the character being refreshed, create an address for the character generator ROM. The output data of the ROM, which is seven parallel bits, represents the display pattern. The Shift Register takes this data and forms the serial video data. The Video Summer combines and buffers the serial video data with CRTC device timing signals to form a composite video output and a separate video, horizontal sync, and vertical sync.

The Program ROM contains the firmware for an intelligent CRT driver, in addition to utilities to aid in custom CRT display application software. There are six predefined screen formats, including 25 lines of 80 characters (50 or 60 Hz), 22 lines of 72 characters (50 or 60 Hz), 25 lines of 40 characters (50 Hz), and 16 lines of 40 characters (60 Hz). For other formats, any dimensions from 1 to 25 lines of from 1 to 80 characters can be defined (50 or 60 Hz). Full screen inverse video and 256 display characters allow flexible display capabilities.

The intelligent display driver controls all screen updating and cursor movement for the selected screen format. The cursor can be on, off, or blinking with movements including up, down, left, right, home, and carriage return, as well as to any row and column position. There are many commands to facilitate screen editing, such as:

- Insert character or line
- Delete character or line
- Clear to end of line
- Clear to end of screen
- Clear line or screen
- Set or Clear special character mode

The firmware utilities are useful for special applications. There is also a display driver which replaces the AIM 65 on-board display with a CRT monitor and an AIM 65 Assembler listing reformatter which takes advantage of the longer display lines.

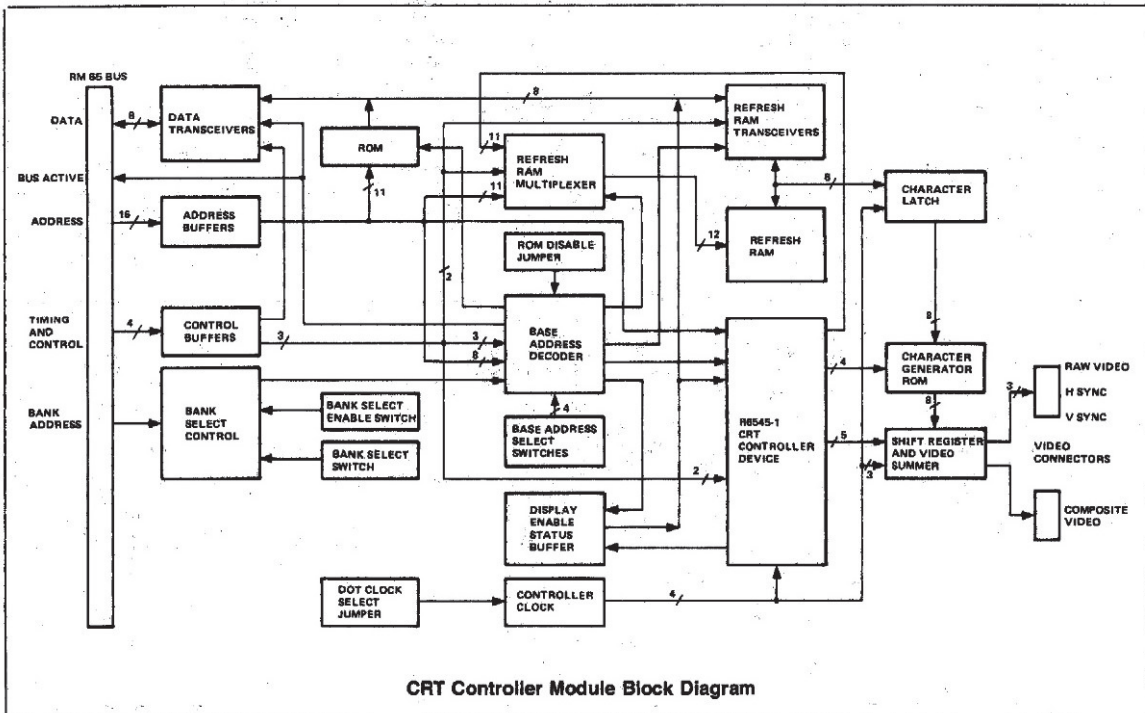
RM 65 CRTC Control Commands

Hex Code	Character	Description	Hex Code	Character	Description
00	CTRL @	*	10	CTRL P	Pass Through Next Character
01	CTRL A	Clear Line	11	CTRL Q	*
02	CTRL B	Clear to End of Line	12	CTRL R	*
03	CTRL C	Clear Screen	13	CTRL S	Toggle Insert Character Mode
04	CTRL D	Clear to End of Screen	14	CTRL T	Delete One Character
05	CTRL E	Clear Screen	15	CTRL U	Insert One Line
06	CTRL F	Clear to End of Screen	16	CTRL V	Delete One Line
07	CTRL G	*	17	CTRL W	Display Cursor
08	CTRL H	Backspace (←)	18	CTRL X	Blank Cursor
09	CTRL I	Horizontal Tab (→)	19	CTRL Y	Relink AIM 65 Display
0A	CTRL J	Line Feed (↓)	1A	CTRL Z	*
0B	CTRL K	Vertical Tab (↓)	1B	CTRL [Escape Character (ESC) (1)
0C	CTRL L	Form Feed (Clear Screen)	1C	CTRL \	Blinking Cursor
0D	CTRL M	Carriage Return (Home on Line)	1D	CTRL]	Enter Normal Characters
0E	CTRL N	Home on Screen	1E	CTRL ^	Perform Self Test
0F	CTRL O	Home on Screen	1F	CTRL _	Reverse Video

*These characters have no effect.

(1) There are two escape sequences as follows:

Hex Code	Character Sequence	Function
1B 3D YY XX	ESC = y x	Move the cursor to the row y and column x position, with row y between top (\$00) and bottom (\$19), and column x between leftmost (\$00) and rightmost (\$4F).
1B 47	ESC G	Enter Graphics Character Mode

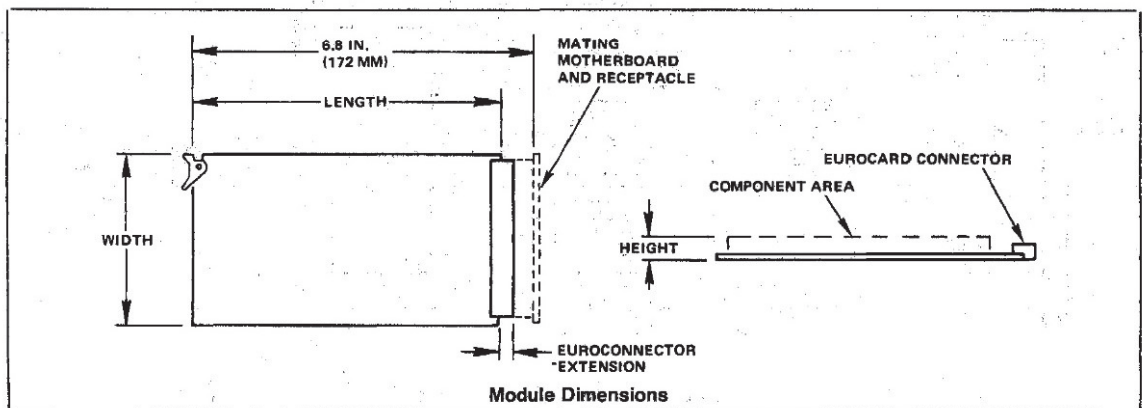


CRT Controller Module Block Diagram

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Pin	Signal Mnemonic	Signal Name	Pin	Signal Mnemonic	Signal Name
1a	GND	Ground	1c	+5V	+5 Vdc
2a	BADR/	Buffered Bank Address	2c	BA15/	Buffered Address Bit 15
3a	GND	Ground	3c	BA14/	Buffered Address Bit 14
4a	BA13/	Buffered Address Bit 13	4c	BA12/	Buffered Address Bit 12
5a	BA11/	Buffered Address Bit 11	5c	GND	Ground
6a	BA10/	Buffered Address Bit 10	6c	BA9/	Buffered Address Bit 9
7a	BA8/	Buffered Address Bit 8	7c	BA7/	Buffered Address Bit 7
8a	GND	Ground	8c	BA6/	Buffered Address Bit 6
9a	BA5/	Buffered Address Bit 5	9c	BA4/	Buffered Address Bit 4
10a	BA3/	Buffered Address Bit 3	10c	GND	Ground
11a	BA2/	Buffered Address Bit 2	11c	BA1/	Buffered Address Bit 1
12a	BA0/	Buffered Address Bit 0	12c	B ϕ 1	*Buffered Phase 1 Clock
13a	GND	Ground	13c	BSYNC	*Buffered Sync
14a	BSO	*Buffered Set Overflow	14c	BDRQ1/	*Buffered DMA Request 1
15a	BRDY	*Buffered Ready	15c	GND	Ground
16a		*User Spare 1	16c	-12V/-V	*-12 Vdc/-V
17a	+12V/+V	*+12 Vdc/+V	17c		*User Spare 2
18a	GND	Ground Line	18c	BFLT/	*Buffered Bus Float
19a	BDMT/	*Buffered DMA Terminate	19c	B ϕ 0	*Buffered External Phase 0 Clock
20a		*User Spare 3	20c	GND	Ground
21a	BR \overline{W} /	*Buffered Read/Write "Not"	21c	BDRQ2/	*Buffered DMA Request 2
22a		*System Spare	22c	BR/W	Buffered Read/Write
23a	GND	Ground	23c	BACT/	Buffered Bus Active
24a	BIRQ/	*Buffered Interrupt Request	24c	BNM/	*Buffered Non-Maskable Interrupt
25a	B ϕ 2/	Buffered Phase 2 "Not" Clock	25c	GND	Ground
26a	B ϕ 2	Buffered Phase 2 Clock	26c	BRES/	Buffered Reset
27a	BD7/	Buffered Data Bit 7	27c	BD6/	Buffered Data Bit 6
28a	GND	Ground	28c	BD5/	Buffered Data Bit 5
29a	BD4/	Buffered Data Bit 4	29c	BD3/	Buffered Data Bit 3
30a	BD2/	Buffered Data Bit 2	30c	GND	Ground
31a	BD1/	Buffered Data Bit 1	31c	BD0/	Buffered Data Bit 0
32a	+5V	+5 Vdc	32c	GND	Ground

Note:
*Not used on this module.



SPECIFICATIONS

Parameter	Value
Dimensions (1, 2, 3) Width Length Height	3.9 in. (100 mm) 6.3 in. (160 mm) 0.56 in. (14 mm)
Environment Operating Temperature Storage Temperature Relative Humidity	0°C to 70°C -40°C to +85°C 0% to 85% (without condensation)
Power Requirements	+5 Vdc \pm 5%, 0.94 A (4.7 W)—Typical 1.30 A (6.8 W)—Maximum
Interface RM 65 Bus Interface I/O Connector Composite Video Raw Video and Sync	64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed) Mini-coax connector (50 ohm SMC type) Mates to Sealectro Part No. 050-024-0000-220 or equivalent 6-pin connector Mates to AMP No. 87159-6 or equivalent
Notes: 1. Height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.). 2. Length does not include the added extension due to the module ejector. 3. Dimensions conform to DIN 41612.	