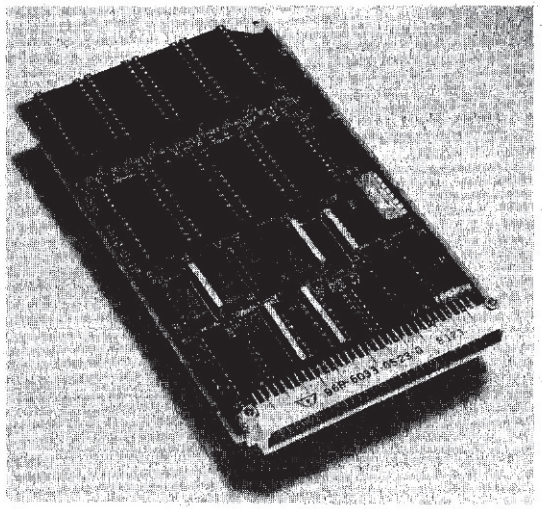
RM65-3264NE
UNIVERSAL MEMORY MODULE

RM 65 MICROCOMPUTER MODULES

The RM65-3264NE Universal Memory Module (16K–128K) is one of the hardware options available for the RM 65 Microcomputer Module Family.

RM 65 Microcomputer Modules are designed for OEM and end user microcomputer applications when state-of-the-art performance, compact size, modular design, and low cost are required. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC, and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 Modules plug into a motherboard designed to accept any card in any slot. The 64-line RM 65 Bus accommodates memory addressing up to 128K bytes, provides high immunity to electrical noise, and includes growth provisions for user functions. A selection of card cages permit packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 or AIM 65/40 Microcomputers for product development and for portable or desktop microcomputer applications.



RM65-3264NE Universal Memory Module

FEATURES

- In the high speed mode, supports Rockwell Design Center 4 MHz RAM operations
- In the universal memory mode, supports 2K, 4K, 8K, and 16K byte-wide memory devices
- On-board header and shunt configure the module into a 2K to 128K memory space
- Each half (four device sockets) independently configurable in the universal memory mode
- On-board memory bank select switches assign each half of the module to either one or both of two 64K memory banks
- On-board ROM select switches serve as write-protect switches for each half of the memory in universal memory mode
- Rockwell RM 65 Bus compatible
- Compact size—100 mm × 167 mm (approximately 4 in. × 6.3 in.)
- Operates from a single +5V power source
- Fully assembled (except for user-supplied memory devices), tested and warranted
- Supports 16K of 2K devices, 32K of 4K devices, 64K of 8K devices, and 128K of 16K devices in universal memory mode
- Supports 64K of 8K devices in high speed mode (refer to Devices Supported for part numbers)

OVERVIEW

Two major capabilities are provided in the Universal Memory Module: the flexibility of using 2K, 4K, 8K, or 16K memory devices on the module, and use of the memory in either a high-speed mode or a universal memory mode. Typical data-transfer rates are up to 4 MHz (to support the Rockwell Design Center (RDC) System) in the high speed mode and 1- to 2-MHz in the universal memory mode. Rates are dependent both on memory devices used and system configuration. Memory devices that can be used with the module are RAM's, ROM's, EPROM's, and EEPROM's.

ORDERING INFORMATION

Part No.	Description
RM65-3264NE	Universal Memory Module

FUNCTIONAL DESCRIPTION

Data Bus Transceivers buffer and invert data signals BD0/ through BD7/. Data signals from the RM 65 Bus pass through the bidirectional transceivers into the module during a write operation and out from the module through the transceivers to the RM 65 Bus during a read operation. Data in is inverted for use in the module, and data out (from the module) is inverted for use on the RM 65 Bus. Transfers occur when any of the chip-select signals and the Ø2 clock pulse are in the active states concurrently. Direction of data flow either into or out of the module is controlled by the R/$\overline{W}$ signal state.

Address and Control Buffer logic consists of inverters that buffer address signals BA0/ through BA13/ and the read/write signal BR/W/. These signals are converted to positive signals BA0 through BA13 and BR/W for use within the module.

Bank Address Select logic is controlled by the state of the BADR/ signal, which functions as a seventeenth address bit. The state of the BADR/ signal indicates which of the two 65K memory banks is addressed. In the high speed memory mode, the module can be configured to operate in either one or both 65K memory banks. In the universal memory mode, each half of the memory is configurable to either one or both 65K memory banks.

Module Active logic is enabled when any chip-select signal is enabled. Thus, when any memory device in either Memory A or Memory B is enabled by a chip-select signal, the BACT/, or Module Active, signal is in the active state.

Address signals BA13/, BA14/, and BA15/, in conjunction with B0, are decoded by a 3:8 decoder to enable one of eight possible outputs. Each output signal in a low state indicates an 8K address boundary signal. Thus, the 8K address boundaries are $0000, $2000, $4000, . . . $E000. Each of these signals is used as a memory chip-select signal during operation of the memory in the high-speed mode and as a 2K, 4K, 8K, and 16K decoder enabling signal in the universal memory mode.

By connecting a pin on the Address Header to a specific output (chip select) pin from the 8K Decoder, that 8K address boundary signal is connected to one specific memory device (in one of the eight memory device sockets) only in high speed mode.

The module can be used either as a high speed memory or as a universal memory. The removable 16-pin 8-position shunt is placed either in the High Speed Option Shunt socket for high speed memory operation, or in the Universal Memory Option Shunt socket for universal memory operation. In the high speed mode, Memory A Decoder and Memory B Decoder are not used, and the address (chip-select) signal from the Address Header is applied directly to the applicable Memory A or Memory B devices. As a result, decoding time is saved.

Memory A consists of 2K, 4K, 8K, or 16K memory devices installed in the four sockets assigned as Memory A. Memory B also consists of memory devices located in four sockets designated as Memory B. Thus, the capacity of Memory A or Memory B is dependent on the capacity of the memory devices installed in each socket. Each of the two groups of four sockets can be configured with jumpers to accept one of the four types (2K, 4K, 8K, or 16K) of memory devices. Each memory device in the memory sockets in Memory A or Memory B must have the same capacity.

Device Select A consists of jumpers E3, E4, and E7 through E10 determine the particular type memory device (2K, 4K, 8K, or 16K) installed in the Memory A sockets. Similarly, Device Select B jumpers E5, E6, and E11 through E14 determine memory device types in Memory B.

Memory A Decoder is a programmable array logic (PAL) device internally configured to decode a combination of input signals and generate one output (chip-select) signal. Memory Decoders A and B are used only when the module is being operated in the universal memory mode. Both decoders operate in the same manner, but only one is used at a time. Thus, when Memory A is addressed, Memory Decoder A is used, and Memory Decoder B when Memory B is addressed.

DEVICES SUPPORTED

In the universal memory mode, the following is a partial list of devices supported:

16K of the following 2K devices:

R2316	ROM-Rockwell
2716	EPROM-Intel
2516	EPROM-TI
2016	RAM-Toshiba
5516	RAM-Toshiba
6116	RAM-Hitachi
R5213/2816	EEPROM-Rockwell
X2816	EEROM-XICOR

32K of the following 4K devices:

R2332	ROM-Rockwell
2732A	ROM-Intel
2532 (350ns)	ROM-TI

64K of the following 8K devices:

R2364A, R2364B	ROM-Rockwell
68A764	EPROM-Motorola
68766	EPROM-Motorola
2764	EPROM-Intel
5564	RAM-Toshiba
6264	RAM-Hitachi
8464	RAM-Fujitsu

128K of the following 16K devices:

R23128	ROM-Rockwell
27128	EPROM-Intel

In the high speed mode, the following is a partial list of devices supported:

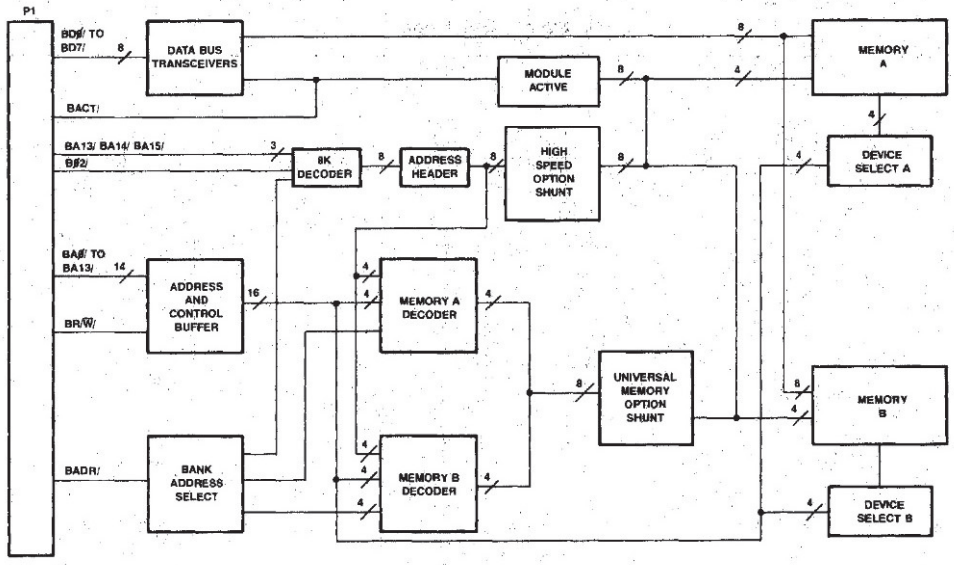
64K of the following 8K devices:

R2364A, R2364B	ROM-Rockwell
68A764	EPROM-Motorola
68766	EPROM-Motorola
2764	EPROM-Intel
5564	RAM-Toshiba
6264	RAM-Hitachi
8464	RAM-Fujitsu

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Pin	Signal Mnemonic	Signal Name	Pin	Signal Mnemonic	Signal Name
1a	GND	Ground	1c	+5V	+5 Vdc
2a	BADR/	Buffered Bank Address	2c	BA15/	Buffered Address Bit 15
3a	GND	Ground	3c	BA14/	Buffered Address Bit 14
4a	BA13/	Buffered Address Bit 13	4c	BA12/	Buffered Address Bit 12
5a	BA11/	Buffered Address Bit 11	5c	GND	Ground
6a	BA10/	Buffered Address Bit 10	6c	BA9/	Buffered Address Bit 9
7a	BA8/	Buffered Address Bit 8	7c	BA7/	Buffered Address Bit 7
8a	GND	Ground	8c	BA6/	Buffered Address Bit 6
9a	BA5/	Buffered Address Bit 5	9c	BA4/	Buffered Address Bit 4
10a	BA3/	Buffered Address Bit 3	10c	GND	Ground
11a	BA2/	Buffered Address Bit 2	11c	BA1/	Buffered Address Bit 1
12a	BA0/	Buffered Address Bit 0	12c	BØ1	*Buffered Phase 1 Clock
13a	GND	Ground	13c	BSYNC	*Buffered Sync
14a	BSO	*Buffered Set Overflow	14c	BDRQ1/	*Buffered DMA Request 1
15a	BRDY	*Buffered Ready	15c	GND	Ground
16a		*User Spare 1	16c	−12V/−V	*−12 Vdc/−V
17a	+12V/+V	*+12 Vdc/+V	17c		*User Spare 2
18a	GND	Ground Line	18c	BFLT/	*Buffered Bus Float
19a	BDMT/	*Buffered DMA Terminate	19c	BØ0	*Buffered External Phase 0 Clock
20a		*User Spare 3	20c	GND	Ground
21a	BR/$\overline{W}$/	Buffered Read/Write "Not"	21c	BDRQ2/	*Buffered DMA Request 2
22a		*System Spare	22c	BR/$\overline{W}$	*Buffered Read/Write
23a	GND	Ground	23c	BACT/	Buffered Bus Active
24a	BIRQ/	*Buffered Interrupt Request	24c	BNMI/	*Buffered Non-Maskable Interrupt
25a	BØ2/	Buffered Phase 2 "Not" Clock	25c	GND	Ground
26a	BØ2	Buffered Phase 2 Clock	26c	BRES/	*Buffered Reset
27a	BD7/	Buffered Data Bit 7	27c	BD6/	Buffered Data Bit 6
28a	GND	Ground	28c	BD5/	Buffered Data Bit 5
29a	BD4/	Buffered Data Bit 4	29c	BD3/	Buffered Data Bit 3
30a	BD2/	Buffered Data Bit 2	30c	GND	Ground
31a	BD1/	Buffered Data Bit 1	31c	BD0/	Buffered Data Bit 0
32a	+5V	+5 Vdc	32c	GND	Ground

Note: *Not used on this module

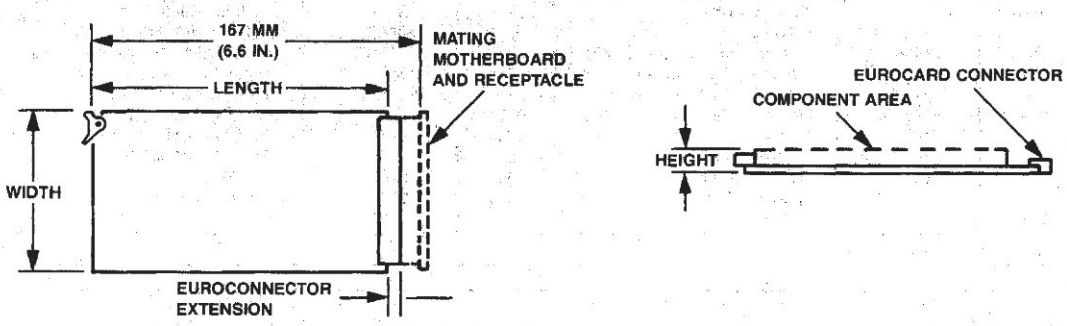


Universal Memory Module Block Diagram

SPECIFICATIONS

Parameter	Value
Dimensions[1,2,3]	
Width	100 mm (3.94 in.)
Length	160 mm (6.3 in.)
Height	14 mm (0.56 in.)
Weight	156 g (5.5 oz.)
Environment	
Operating Temperature	0°C to 70°C
Storage Temperature	−40°C to 85°C
Relative Humidity	0% to 85% (without condensation)
Power Requirements	5.0V (420 ma. typical, 640 ma. maximum with no memory devices installed)
Connector	
RM 65 Bus Connector P1	64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed)—mates with Burndy P196B32R00A00L-9 or equivalent.

Notes:
1. Height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. Length does not include the added extension due to the module ejector.
3. Dimensions conform to DIN 41612.



Module Dimensions