Rockwell

RM65-3216E
RM 65 16K PROM/ROM MODULE

RM 65 MICROCOMPUTER MODULES

The RM65-3216E 16K PROM/ROM Module is one of the hardware options available for the RM 65 Microcomputer Module family.

RM 65 Microcomputer Module products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 module products use a motherboard interconnect concept and accept any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and for a broad variety of portable or desktop microcomputer applications.

PRODUCT OVERVIEW

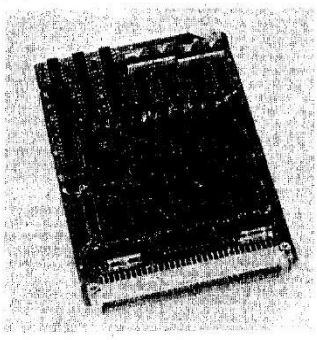
The RM 65 16K PROM/ROM Module has eight, 24-pin sockets to accept up to 16K bytes of either programmable read-only memory (PROM) or masked read-only memory (ROM) devices. On-board jumpers permit selection of 2K, 4K or 8K byte PROM/ROM devices. Switches allow setting of the starting address for independent 4K byte blocks of memory. All 16K bytes can be assigned to two memory banks, or 8K can be assigned to common memory while the other 8K can be dedicated to one or two 65K memory banks. Low power operation is jumper selectable for PROMs that have this option.

FEATURES

- Compact size—about 4" × 6¼" (100 mm × 160 mm)
- Pin and socket bus connection
- RM 65 Bus compatible
- Buffered address, data and control lines
- Supports the following PROMs/ROMs or equivalents:
  Intel 2716 or 2732 PROMs
  TI TMS 2516 or 2532 PROMs
  Rockwell R2316, R2332 or R2364 ROMs
- Low-power PROM operation selectable by individual socket jumpers
- Jumpers allow selection of 2K, 4K or 8K byte devices
- Starting address selectable for each of four 4K memory blocks
- Separate switch allows 8K to be dedicated to one or two memory bank operation
- +5V operation
- Fully assembled, tested and warranted

ORDERING INFORMATION

Part No.	Description
RM65-3216E	16K PROM/ROM Module
Order No.	**Description**
806	16K PROM/ROM Module User's Manual (included with RM65-3216E)



RM65-3216E 16K PROM/ROM Module

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FUNCTIONAL DESCRIPTION

The PROM/ROM module has eight 24-pin sockets which can accept up to 16K of either 2K, 4K, or 8K PROM or ROM.

The Data Buffers invert and transfer 8-bits of parallel data from the selected PROM/ROM devices to the RM 65 Bus during read operations.

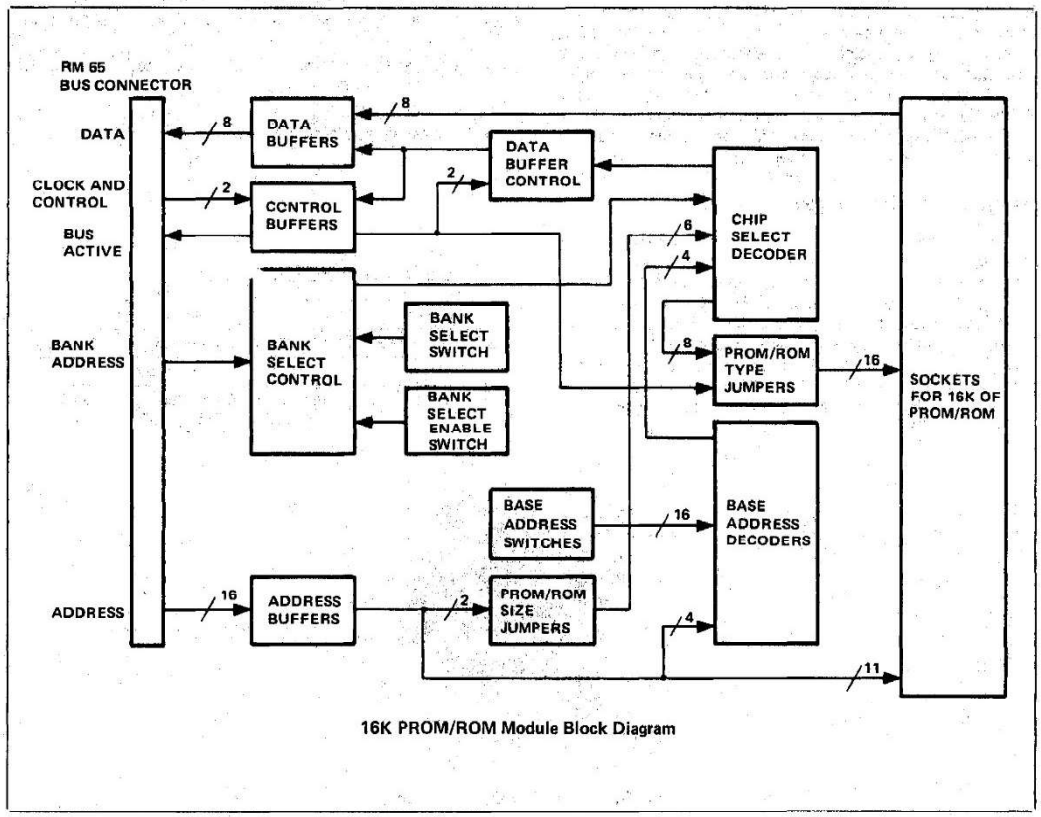
The Control Buffers invert and transfer phase 2 clock, and read/write control signals from the RM 65 Bus onto the PROM/ROM module, and drive the bus active signal onto the RM 65 Bus.

The Bank Select control circuit detects when the PROM/ROM module's assigned memory bank is addressed, by comparing the bank address signal from the RM 65 Bus to the Bank Select and Bank Select Enable switches. The Bank Select Enable switch allows 8K of the PROM/ROM to be common memory (addressable in both Bank 0 and Bank 1) while the remaining 8K is assigned either to Bank 0 or Bank 1, as determined by the Bank Select switch.

Four Base Address Decoders allow 4K PROM/ROM sections to be independently addressed on any 4K boundary within the selected bank. When an address falls within any section (per the Base Address switches), an enable signal is sent to the Chip Select Decoder.

The Chip Select Decoder uses outputs from the Bank Select Control circuit, the Base Address Decoders, and the PROM/ROM size jumpers as well as the address lines to generate chip selects to the PROM/ROM devices. The PROM/ROM type jumpers route the chip select lines to the correct pins on the PROM/ROM sockets.

The Data Buffer Control circuit enables the Data Buffers during a read operation when an address corresponding to a selected base address is decoded and the selected PROM/ROM memory bank is addressed.



16K PROM/ROM Module Block Diagram

RM 65 Bus Pin Assignments

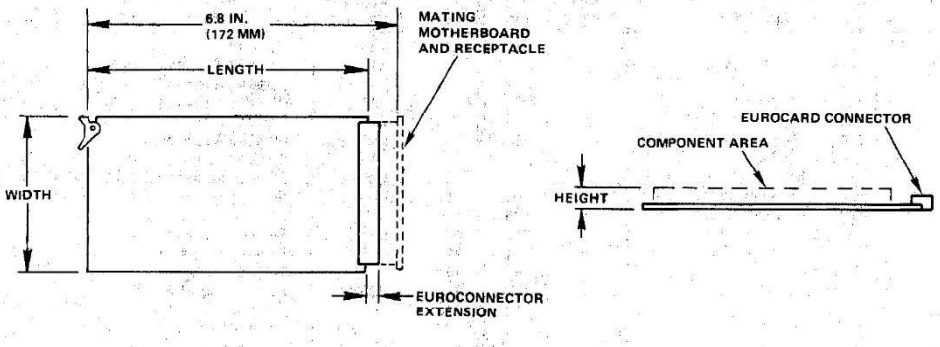
Bottom (Solder Side)				Top (Component Side)			
Signal Mnemonic	Signal Name	Input/ Output	Pin	Pin	Signal Mnemonic	Signal Name	Input/ Output
GND	Ground		1a	1c	+5V	+5 Vdc	
BADR/	Buffered Bank Address	I	2a	2c	BA15/	Buffered Address Bit 15	I
GND	Ground		3a	3c	BA14/	Buffered Address Bit 14	I
BA13/	Buffered Address Bit 13	I	4a	4c	BA12/	Buffered Address Bit 12	I
BA11/	Buffered Address Bit 11	I	5a	5c	GND	Ground	
BA10/	Buffered Address Bit 10	I	6a	6c	BA9/	Buffered Address Bit 9	I
BA8/	Buffered Address Bit 8	I	7a	7c	BA7/	Buffered Address Bit 7	I
GND	Ground		8a	8c	BA6/	Buffered Address Bit 6	I
BA5/	Buffered Address Bit 5	I	9a	9c	BA4/	Buffered Address Bit 4	I
BA3/	Buffered Address Bit 3	I	10a	10c	GND	Ground	
BA2/	Buffered Address Bit 2	I	11a	11c	BA1/	Buffered Address Bit 1	I
BA0/	Buffered Address Bit 0	I	12a	12c	BØ1	*Buffered Phase 1 Clock	
GND	Ground		13a	13c	BSYNC	*Buffered Sync	
BSO	*Buffered Set Overflow		14a	14c	BDRQ1/	*Buffered DMA Request 1	
BRDY	*Buffered Ready		15a	15c	GND	Ground	
	*User Spare 1		16a	16c	−12V/−V	*−12 Vdc/−V	
+12V/+V	*+12 Vdc/+V		17a	17c		*User Spare 2	
GND	Ground Line		18a	18c	BFLT/	*Buffered Bus Float	
BDMT/	*Buffered DMA Terminate		19a	19c	BØ0	*Buffered External Phase 0 Clock	
	*User Spare 3		20a	20c	GND	Ground	
BR/$\overline{W}$/	*Buffered Read/Write "Not"	I	21a	21c	BDRQ2/	*Buffered DMA Request 2	
	*System Spare		22a	22c	BR/$\overline{W}$	Buffered Read/Write	I
GND	Ground		23a	23c	BACT/	Buffered Bus Active	O
BIRQ/	*Buffered Interrupt Request		24a	24c	BNMI/	*Buffered Non-Maskable Interrupt	
BØ2/	*Buffered Phase 2 "Not" Clock		25a	25c	GND	Ground	
BØ2	*Buffered Phase 2 Clock		26a	26c	BRES/	*Buffered Reset	
BD7/	Buffered Data Bit 7	O	27a	27c	BD6/	Buffered Data Bit 6	O
GND	Ground		28a	28c	BD5/	Buffered Data Bit 5	O
BD4/	Buffered Data Bit 4	O	29a	29c	BD3/	Buffered Data Bit 3	O
BD2/	Buffered Data Bit 2	O	30a	30c	GND	Ground	
BD1/	Buffered Data Bit 1	O	31a	31c	BD0/	Buffered Data Bit 0	O
	Not Connected (See Note)		Za	Zc		Not Connected (See Note)	

Note:
*Not used on the 16K PROM/ROM module.

SPECIFICATIONS

Parameter	Value
Dimensions (1, 2, 3)	
Width	3.9 in. (100 mm)
Length	6.3 in. (160 mm)
Height	0.56 in. (14 mm)
Weight	5.0 oz. (140 g)
Environment	
Operating Temperature	0°C to 70°C
Storage Temperature	−40°C to +85°C
Relative Humidity	0% to 85% (without condensation)
Power Requirements	
w/o PROM/ROM Devices	+5 Vdc ±5% 0.17A (0.85W)—Typical 0.27A (1.35W)—Maximum
Access Time	450 nanoseconds (max)
RM 65 Bus Interface	
Edge Connector Version	72-pin edge connector (0.100 in. centers)
Eurocard Version	64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed)

Notes:
1. Height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. Length does not include the added extension due to the module ejector.
3. Dimensions conform to DIN 41612.



Module Dimensions