Rockwell

RM65-3108E
RM 65 8K STATIC RAM MODULE

RM 65 MICROCOMPUTER MODULES

The RM65-3108E 8K Static RAM Module is one of the hardware options available for the RM 65 Microcomputer Module family.

RM 65 Microcomputer Module products are designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

RM 65 module products use a motherboard interconnect concept and accept any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell AIM 65 and AIM 65/40 Microcomputers for product development and for a broad variety of portable or desktop microcomputer applications.

PRODUCT OVERVIEW

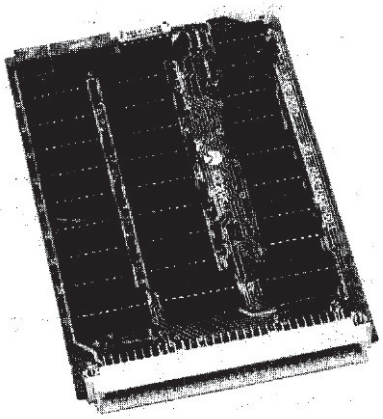
The RM65-3108E 8K Static RAM Module contains 8192 8-bit bytes of Random Access Memory (RAM), in sixteen 2114 static RAM devices. The memory is arranged as two separately addressable 4K memory sections. The starting address of each 4K section is selectable by on-board address switches. A Bank Select switch allows the RAM module to be assigned to one of two 64K memory banks.

FEATURES

- Compact size—about 4" × 6¼" (100 mm × 160 mm)
- Pin and socket bus connectors
- RM 65 Bus compatible
- Buffered address, data and control lines
- Two separately addressable 4K byte sections
- 16 socketed 2114 static RAM devices
- Write-protect switch for each memory section
- Bank Select and Enable switches
- +5V operation
- Fully assembled, tested and warranted.

ORDERING INFORMATION

Part No.	Description
RM65-3108E RM65-3108NE	8K Static RAM Module 8K Static RAM Module (without RAM devices installed)
Order No.	**Description**
805	8K Static RAM Module User's Manual (included with RM65-3108E and RM65-3108NE)



RM65-3108E 8K Static RAM Module

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FUNCTIONAL DESCRIPTION

8K bytes of static 2114 RAM are divided into two separately addressable 4K blocks. Two devices per 1K bytes are required since each device is 1K × 4 bits.

The Data Transceivers invert and transfer 8-bits of parallel data between the RAM devices and the RM 65 Bus, based on data direction signals from the Data Transceiver Control Circuit.

The Address Buffers invert and transfer 16 address bits from the RM 65 Bus to the RAM devices, to the Base Address Decoders and to the Chip Select Decoder.

The Control Buffers invert and transfer phase 2 clock and read/write control signals from the RM 65 Bus onto the RAM module, and drive the bus active signal onto the RM 65 Bus.

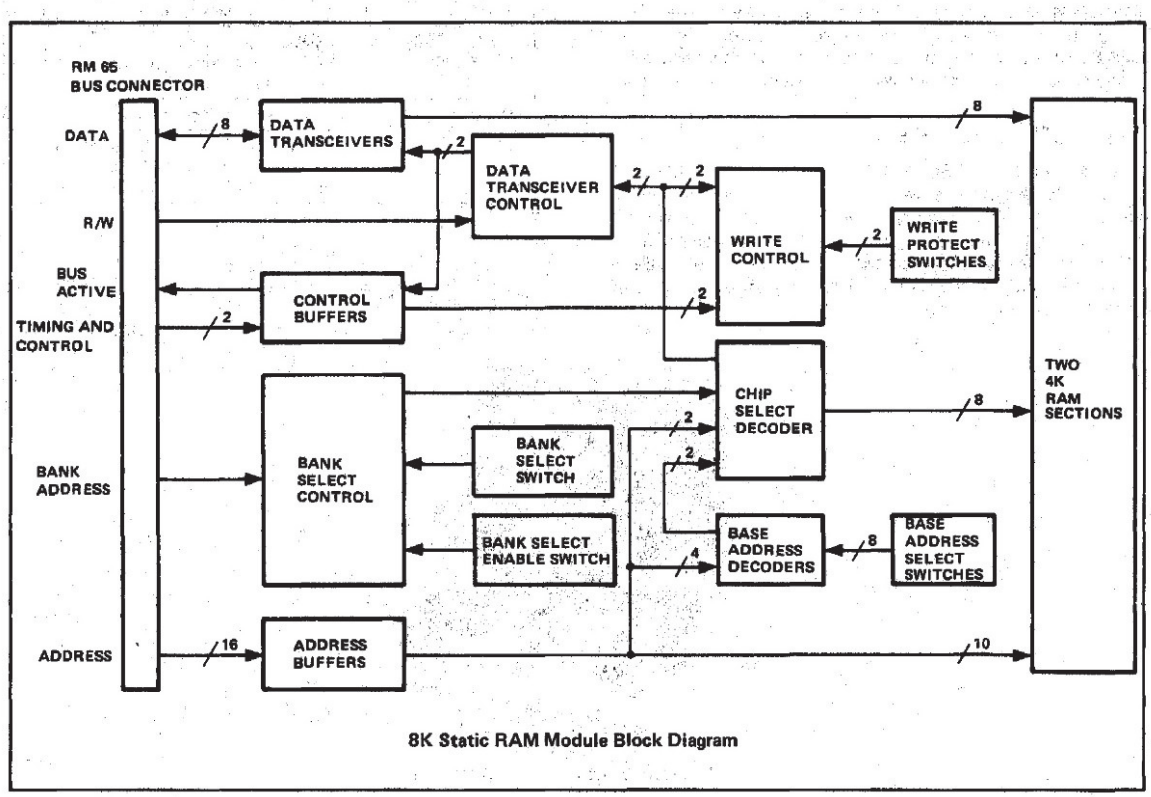
The Bank Select Controller detects when the RAM module's assigned memory bank is addressed, by comparing the bank address signal from the RM 65 Bus to the settings of the Bank Select and Bank Select Enable switches. If the addressed bank is the same as the selected memory bank, an enable signal is sent to the Chip Select Decoder.

Two Base Address Decoders detect when either 4K RAM Section (1 or 2) is addressed, by comparing the address lines to Base Address Select switch settings. When a match occurs, an enable signal is sent to the Chip Select Decoder.

The Chip Select Decoder uses outputs from the Bank Select Control circuit, the Base Address Decoders, and the PROM/ROM size jumpers as well as address lines A11 and A10 to generate one of eight chip select lines to the RAM devices. A signal indicating that a chip select line is active is also sent to the Write Control and Data Transceiver Control circuits.

The Write Control circuit generates the write enable signals to the RAM devices and to the Data Transceiver Control circuit. If the corresponding write protect switch is off, the write enable signal is activated. If the Write Protect switch is on, the Data Transceivers are disabled.

The Data Transceiver Control circuit determines whether a valid read or write operation is in progress, and provides transceiver enable and data direction signals to the Data Transceivers. The Data Transceivers are enabled if both the bank address and the address lines correspond to the selected bank and a selected base address, respectively.

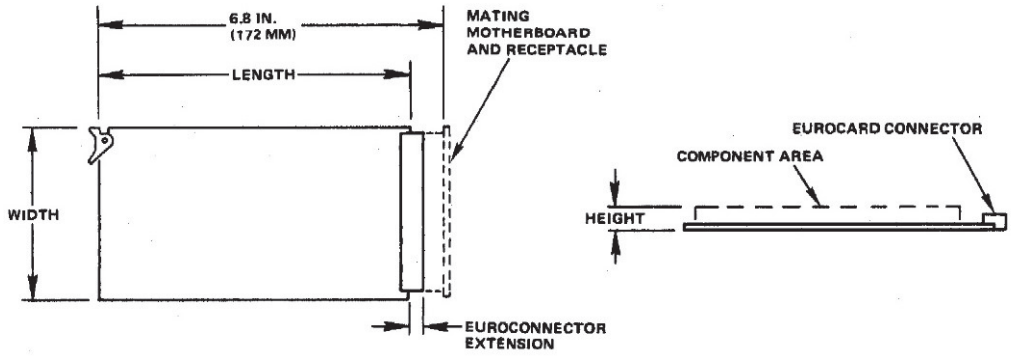


8K Static RAM Module Block Diagram

RM 65 Bus Pin Assignments

Bottom (Solder Side)				Top (Component Side)			
Pin	Signal Mnemonic	Signal Name	Input/ Output	Pin	Signal Mnemonic	Signal Name	Input/ Output
1a	GND	Ground		1c	+5V	+5 Vdc	
2a	BADR/	Buffered Bank Address	I	2c	BA15/	Buffered Address Bit 15	I
3a	GND	Ground		3c	BA14/	Buffered Address Bit 14	I
4a	BA13/	Buffered Address Bit 13	I	4c	BA12/	Buffered Address Bit 12	I
5a	BA11/	Buffered Address Bit 11	I	5c	GND	Ground	
6a	BA10/	Buffered Address Bit 10	I	6c	BA9/	Buffered Address Bit 9	I
7a	BA8/	Buffered Address Bit 8	I	7c	BA7/	Buffered Address Bit 7	I
8a	GND	Ground		8c	BA6/	Buffered Address Bit 6	I
9a	BA5/	Buffered Address Bit 5	I	9c	BA4/	Buffered Address Bit 4	I
10a	BA3/	Buffered Address Bit 3	I	10c	GND	Ground	
11a	BA2/	Buffered Address Bit 2	I	11c	BA1/	Buffered Address Bit 1	I
12a	BA0/	Buffered Address Bit 0	I	12c	Bø1	*Buffered Phase 1 Clock	
13a	GND	Ground		13c	BSYNC	*Buffered Sync	
14a	BSO	*Buffered Set Overflow		14c	BDRQ1/	*Buffered DMA Request 1	
15a	BRDY	*Buffered Ready		15c	GND	Ground	
16a		*User Spare 1		16c	−12V/−V	*−12 Vdc/−V	
17a	+12V/+V	*+12 Vdc/+V		17c		*User Spare 2	
18a	GND	Ground Line		18c	BFLT/	*Buffered Bus Float	
19a	BDMT/	*Buffered DMA Terminate		19c	Bø0	*Buffered External Phase 0 Clock	
20a		*User Spare 3		20c	GND	Ground	
21a	BR/$\overline{W}$/	Buffered Read/Write "Not"	I	21c	BDRQ2/	*Buffered DMA Request 2	
22a		*System Spare		22c	BR/$\overline{W}$	Buffered Read/Write	I
23a	GND	Ground		23c	BACT/	Buffered Bus Active	O
24a	BIRQ/	*Buffered Interrupt Request		24c	BNMI/	*Buffered Non-Maskable Interrupt	
25a	Bø2/	Buffered Phase 2 "Not" Clock	I	25c	GND	Ground	
26a	Bø2	*Buffered Phase 2 Clock		26c	BRES/	*Buffered Reset	
27a	BD7/	Buffered Data Bit 7	I/O	27c	BD6/	Buffered Data Bit 6	I/O
28a	GND	Ground		28c	BD5/	Buffered Data Bit 5	I/O
29a	BD4/	Buffered Data Bit 4	I/O	29c	BD3/	Buffered Data Bit 3	I/O
30a	BD2/	Buffered Data Bit 2	I/O	30c	GND	Ground	
31a	BD1/	Buffered Data Bit 1	I/O	31c	BD0/	Buffered Data Bit 0	I/O
32a	+5V	+5 Vdc		32c	GND	Ground	

Note:
*Not used on this module.



Module Dimensions

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SPECIFICATIONS

Parameter	Value
Dimensions (See Notes) Width Length Height	 3.9 in. (100 mm) 6.3 in. (160 mm) 0.56 in. (14 mm)
Weight	5.3 oz. (145 g)
Environment Operating Temperature Storage Temperature Relative Humidity	 0°C to 70°C −40°C to +85°C 0% to 85% (Without condensation)
Power Requirements	+5 Vdc ±5% @ 1.0A (5.0W)—Typical 1.9A (9.5W)—Maximum
Access Time	450 ns—Maximum
RM 65 Bus Interface	64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed)

Notes:
1. Height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. Length does not include the added extension due to the module ejector.
3. Dimensions conform to DIN 41612.