PART NUMBER
RM65-1000(E)

Rockwell

RM 65
DATA SHEET

SINGLE BOARD COMPUTER (SBC) MODULE

RM 65

The RM 65 product line is designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

The RM 65 product line uses a motherboard interconnect concept and accepts any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell's AIM 65 Microcomputer for product development and for a broad variety of portable or desktop microcomputer applications.

PRODUCT OVERVIEW

The Single Board Computer Module (SBC) allows users to design their products into compact modular stacks. The SBC module plugs into a single slot in an RM 65 card cage/motherboard and controls other memory and I/O modules. The heart of the SBC module is an R6502 CPU, which is capable of addressing 65K bytes of memory. In addition, the SBC module contains bank address logic which allows addressing of one or two 65K byte memory banks. Sockets on the module accept up to 16K bytes of PROM/ROM. 2K bytes of static RAM are also provided.

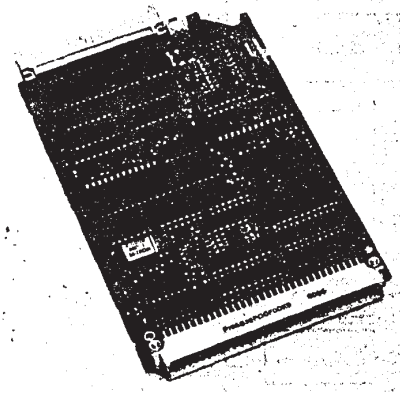
An R6522 Versatile Interface Adapter (VIA) provides two 8-bit parallel I/O data lines, two 2 bit control lines, two counter-timers and an 8-bit shift register. On-board switches assign memory sections to 4K byte blocks. All address, data and control lines are buffered.

FEATURES

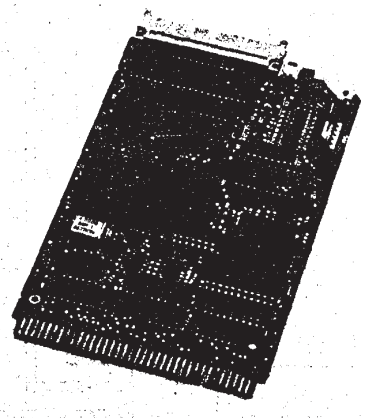
- Compact size – about 4" x 6½" (100 mm x 160 mm)
- Edge connector and Eurocard versions
- On-board R6502 CPU
- 2K of 2114 static RAM
- Two sockets for up to 16K PROM/ROM
- Supports the following PROM/ROM or equivalents
  - TI TMS 2516, TMS 2532 and Motorola MCM68764 PROMs
  - Rockwell R2316, R2332, or R2364 ROMs
- R6522 Versatile Interface Adapter (VIA) and I/O Interface
- Fully Buffered Address, Data, and Control lines for RM 65 Bus
- Separate switches allow RAM, PROM/ROM, and VIA to be individually dedicated to one or two 65K byte memory banks
- Jumpers allow selection of the following
  - 2K, 4K or 8K PROM/ROMs
  - RAM, PROM/ROM and I/O starting address to 4K byte boundary
  - On-board or External bank addressing source
  - Programmable DMA Terminate
  - On-board or external clock source
- +5V operation
- Fully assembled, tested and warranted

ORDERING INFORMATION

The SBC Module is available in an Edge Connector version (RM65-1000) and a Eurocard version (RM65-1000E).



Eurocard Version
RM65-1000E



Edge Connector Version
RM65-1000

SINGLE BOARD COMPUTER (SBC) MODULE

RM65 BOARD PRODUCTS

Specifications subject to change without notice
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FUNCTIONAL DESCRIPTION

The Clock Circuit uses a crystal-controlled oscillator to provide a stable 1-MHz clock reference. A jumper selects between the internal clock reference or an external clock (to 1 MHz) as the source for the R6502 and the derived system clock.

The Reset Control circuit conditions the Reset signal to drive the R6502 Reset line. A reset can be generated by either the on-board reset pushbutton or an external switch. This circuitry also generates a reset automatically, upon power-up.

The R6502 Central Processing Unit (CPU) is the heart of the SBC Module and any interfacing Modules connected to the RM 65 Bus. The R6502 controls all program execution by means of the address, data, control, and timing lines. All internal R6502 operations are synchronized to the clock source.

The Bank Select Control circuit detects when the SBC Module's assigned memory bank is addressed, by comparing the Bank Address signal to the Bank Select Enable and Bank Select switches. The Bank Select Enable Switches allow all on-board PROM/ROM, RAM, & VIA to be independently assigned common to both Bank 0 (lower 65K) and Bank 1 (upper 65K) or dedicated to either Bank 0 or Bank 1, depending on the Bank Select switches. A jumper allows the Bank Address signal to be driven by the on-board R6522 VIA or from another module.

The Base Address Decoder uses the six most-significant address bits and the Base Address Jumpers to generate chip selects for the on-board PROM/ROM, RAM, and VIA. The RAM and VIA can be independently mapped into any 4K block of the selected 65K bank. The PROM/ROMs may be mapped into any 4K or 8K block of the selected bank.

The 16K PROM/ROM section has two sockets which can accept 2K, 4K or 8K PROM/ROM devices. The size and type of PROM or ROM is specified by the Base Address selection jumpers and the PROM/ROM type jumpers.

The 2K RAM section uses four 1K x 4 RAM devices to provide on-board read/write memory.

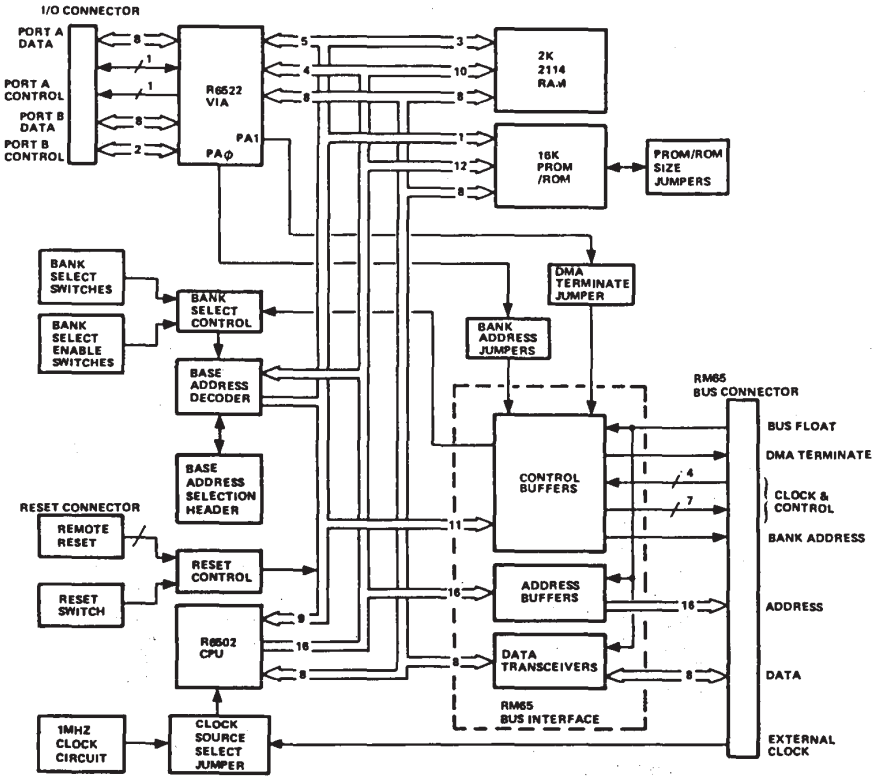
The R6522 Versatile Interface Adapter (VIA) provides input-output capability to the SBC Module. The VIA provides two 8-bit I/O ports each with two control lines. Both ports and control lines are brought out to a connector for user applications.

The SBC Module can control up to 15 additional support modules by means of the RM 65 Bus. There are three groups of signals on the RM 65 Bus: data, address, and control.

The Data Transceivers invert and transfer eight bits of parallel data between the SBC Module and the RM 65 bus. The direction of the transceivers is controlled by the read/write signal from the R6502. The transceivers are disabled when the on-board PROM/ROM RAM, or VIA is addressed or when the Bus Float signal from the RM 65 Bus is active.

The Address Buffers invert and transfer 16 parallel address bits from the SBC Module to the RM 65 bus.

The Control Buffers buffer all control and clock signals between the SBC Module and the RM 65 bus. The Non-Maskable Interrupt, Interrupt Request, Set Overflow, External Clock (Ø0), Ready and Bus Float input lines are buffered coming from the RM 65 bus into the SBC Module. The DMA Terminate, Reset and Phase 1 Clock (Ø1) output lines are always driven from the SBC Module onto the RM 65 Bus. The other six output lines for Read/Write, Phase 2 Clock, sync, and Bank Address are also buffered, but are tri-stated (disabled) when the Bus Float signal is active.



SBC Block Diagram

RM 65 Bus Pin Assignments

Bottom (Solder Side)			Top (Component Side)		
Signal Mnemonic	Signal Name	Pin	Pin	Signal Mnemonic	Signal Name
	Not Connected (See Note)	Wa	Wc		Not Connected (See Note)
+5V	+5 Vdc Line (See Note)	Xa	Xc	+5V	+5-Vdc (See Note)
GND	Ground	1a	1c	+5V	+5 Vdc
BADR/	Buffered Bank Address	2a	2c	BA15/	Buffered Address Bit 15
GND	Ground	3a	3c	BA14/	Buffered Address Bit 14
BA13/	Buffered Address Bit 13	4a	4c	BA12/	Buffered Address Bit 12
BA11/	Buffered Address Bit 11	5a	5c	GND	Ground
BA10/	Buffered Address Bit 10	6a	6c	BA9/	Buffered Address Bit 9
BA8/	Buffered Address Bit 8	7a	7c	BA7/	Buffered Address Bit 7
GND	Ground	8a	8c	BA6/	Buffered Address Bit 6
BA5/	Buffered Address Bit 5	9a	9c	BA4/	Buffered Address Bit 4
BA3/	Buffered Address Bit 3	10a	10c	GND	Ground
BA2/	Buffered Address Bit 2	11a	11c	BA1/	Buffered Address Bit 1
BA0/	Buffered Address Bit 0	12a	12c	BØ1	Buffered Phase 1 Clock
GND	Ground	13a	13c	BSYNC	Buffered Sync
BSO	Buffered Set Overflow	14a	14c	BDRQ1/	*Buffered DMA Request 1
BRDY	Buffered Ready	15a	15c	GND	Ground
	* User Spare 1	16a	16c	-12V/-V	* -12 Vdc/-V
+12V/+V	* +12 Vdc/+V	17a	17c		* User Spare 2
GND	Ground Line	18a	18c	BFLT/	Buffered Bus Float
BDMT/	Buffered DMA Terminate	19a	19c	BØ0	Buffered External Phase 0 Clock
	* User Spare 3	20a	20c	GND	Ground
BR/$\overline{W}$/	Buffered Read/Write "Not"	21a	21c	BDRQ2/	*Buffered DMA Request 2
	* System Spare	22a	22c	BR/$\overline{W}$	Buffered Read/Write
GND	Ground	23a	23c	BACT/	* Buffered Bus Active
BIRQ/	Buffered Interrupt Request	24a	24c	BNMI/	Buffered Non-Maskable Interrupt
BØ2/	Buffered Phase 2 "Not" Clock	25a	25c	GND	Ground
BØ2	Buffered Phase 2 Clock	26a	26c	BRES/	Buffered Reset
BD7/	Buffered Data Bit 7	27a	27c	BD6/	Buffered Data Bit 6
GND	Ground	28a	28c	BD5/	Buffered Data Bit 5
BD4/	Buffered Data Bit 4	29a	29c	BD3/	Buffered Data Bit 3
BD2/	Buffered Data Bit 2	30a	30c	GND	Ground
BD1/	Buffered Data Bit 1	31a	31c	BD0/	Buffered Data Bit 0
+5V	+5 Vdc	32a	32c	GND	Ground
+5V	+5 Vdc (See Note)	Ya	Yc	+5V	+5 Vdc (See Note)
	Not Connected (See Note)	Za	Zc		Not Connected (See Note)

NOTE

Pins Wa, Wc, Xa, Xc, Ya, Yc, Za and Zc are not used on Eurocard version.

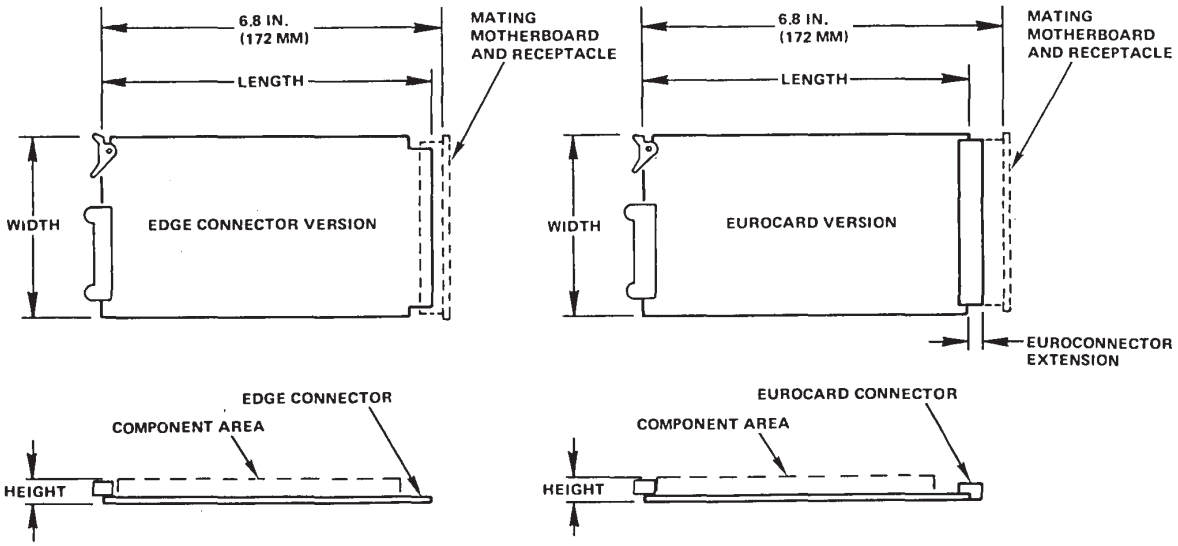
* Not used on this module.

SBC Module Physical and Electrical Characteristics

Characteristic	Value	
Physical characteristics (See Notes)	Edge Connector Version	Eurocard Version
Width	3.9 in. (100 mm)	3.9 in. (100 mm)
Length	6.5 in. (164 mm)	6.3 in. (160 mm)
Height	0.56 in. (14 mm)	0.56 in. (14 mm)
Weight	5.3 oz. (150 g)	5.6 oz. (160 g)
Environment		
Operating Temperature	$0^{o}C$ to $70^{o}C$	
Storage Temperature	$-40^{o}C$ to $+85^{o}C$	
Relative Humidity	0% to 85% (without condensation)	
Power Requirements	+5 Vdc ±5%, 0.75 A (3.5 W) – Typical 1.2 A (6.0 W) – Maximum	
RM 65 Bus Interface		
Edge Connector Version	72-pin edge connector (0.100 in. centers)	
Eurocard Connector Version	64-pin plug (0.100 in. centers) per DIN 41612 (Row B not installed)	
I/O Connector	40-pin 3M mass termination (0.100 in. centers)	
RESET Switch Connector	2 vertical pins (0.3 in. high) on 0.200 in. center	

NOTES:

1. The height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. The length does not include extensions beyond the edge of the module due to connectors or the module ejector.
3. The Eurocard dimensions conform to DIN 41612.



Module Dimensions