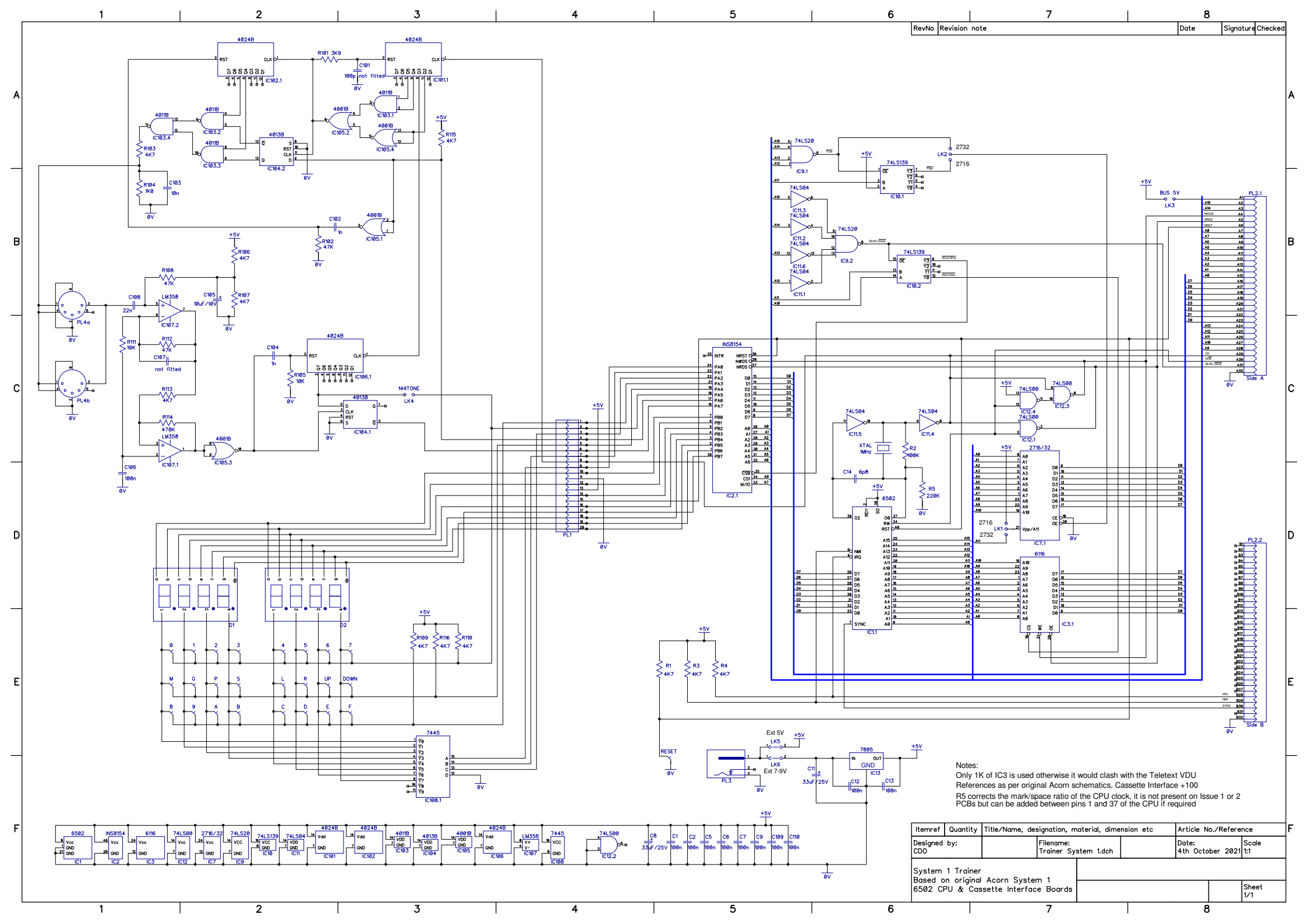
RevNo
Revision note
Date
Signature
Checked
4024B
4011B
4013B
4001B
74LS20
74LS139
74LS04
74LS00
INS8154
6502
2716/32
6116
7445
7805
LM358
PL1
PL2.1
PL2.2
PL4a
PL4b
Side A
Side B
BUS 5V
NMITONE
RESET
XTAL 1MHz
Ext 5V
Ext 7-9V
2732
2716
R101 3K9
R102 47K
R103 4K7
R104 1K0
R105 10K
R106 4K7
R107 4K7
R108 47K
R109 4K7
R110 4K7
R111 10K
R112 47K
R113 4K7
R114 470K
R115 4K7
R116 4K7
R1 4K7
R2 100K
R3 4K7
R4 4K7
R5 220K
C101 100p not fitted
C102 1n
C103 10n
C104 1n
C105 10uF/10V
C106 100n
C107 not fitted
C108 22n
C109 100n
C110 100n
C11 33uF/25V
C12 100n
C13 100n
C14 6p8
C1 100n
C2 100n
C5 100n
C6 100n
C7 100n
C8 33uF/25V
C9 100n
D1
D2
IC1.1
IC2.1
IC3.1
IC7.1
IC9.1
IC9.2
IC10.1
IC10.2
IC11.1
IC11.2
IC11.3
IC11.4
IC11.5
IC11.6
IC12.1
IC12.2
IC12.3
IC12.4
IC13
IC101
IC102
IC103.1
IC103.2
IC103.3
IC103.4
IC104.1
IC104.2
IC105.1
IC105.2
IC105.3
IC105.4
IC106.1
IC107.1
IC107.2
IC108.1
LK1
LK2
LK3
LK4
LK5
LK6
0 1 2 3 4 5 6 7
M G P S L R UP DOWN
8 9 A B C D E F
Notes:
Only 1K of IC3 is used otherwise it would clash with the Teletext VDU
References as per original Acorn schematics, Cassette Interface +100
R5 corrects the mark/space ratio of the CPU clock, it is not present on Issue 1 or 2 PCBs but can be added between pins 1 and 37 of the CPU if required
Itemref
Quantity
Title/Name, designation, material, dimension etc
Article No./Reference
Designed by: CDO
Filename: Trainer System 1.dch
Date: 4th October 2021
Scale 1:1
System 1 Trainer
Based on original Acorn System 1
6502 CPU & Cassette Interface Boards
Sheet 1/1